EXHIBIT 4

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 7,619,912

Issued: November 17, 2009

Filed: September 27, 2007

Inventors: Jayesh R. Bhakta and Jeffrey C. Solomon

Title: MEMORY MODULE DECODER

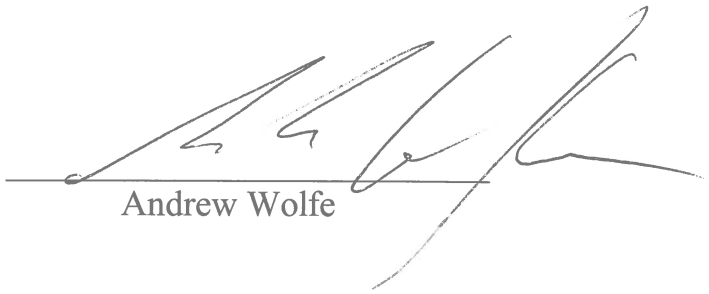
Inter Partes Review No. IPR2022-00615

EXPERT DECLARATION OF DR. ANDREW WOLFE IN SUPPORT OF SAMSUNG ELECTRONICS CO., LTD.'S PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,619,912

Declaration of Dr. Andrew Wolfe Regarding U.S. Patent No. 7,619,912

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: February 17, 2022



Andrew Wolfe

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Petitioner Samsung Electronics Co., Ltd. as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent 7,619,912 ("the '912 Patent") (EX1001) and on the patentability of claim 16 of this patent. The following is my written report on these topics.

B. Background and Qualifications

2. My professional qualifications, experience, publications and presentations, and a listing of previous cases in which I have provided expert testimony are set forth in my CV, attached as Exhibit 1004.

3. I am the founder and sole employee of Wolfe Consulting. Through Wolfe Consulting, I provide technical and business analytics to businesses on processor technology, computer systems, consumer electronics, software, design tools, data security, cryptography and intellectual property issues. I have more than thirty years' experience developing products, researching, consulting, and teaching in those fields. In that time, I have worked as a computer architect, computer system designer, and as an executive in the PC and electronics business. I have also taught at some of the world's leading institutions in those fields, including Stanford University, Princeton University, Carnegie Mellon University, and Santa Clara University.

4. In 1985, I earned the B.S.E.E. degree in Electrical Engineering and Computer Science from the Johns Hopkins University. In 1987, I received the M.S. degree in Electrical and Computer Engineering from Carnegie Mellon University and in 1992, I received the Ph.D. degree in Computer Engineering from Carnegie Mellon University. My doctoral dissertation proposed a new approach for the architecture of a computer processor.

5. I have more than 35 years of experience as a computer architect, computer system designer, personal computer graphics designer, educator, and executive in the electronics industry.

6. In 1983, I began designing touch sensors, microprocessor-based computer systems, and I/O (input/output) cards for personal computers as a senior design engineer for Touch Technology, Inc. During the course of my design projects with Technology, I designed I/O cards for PC-compatible computer systems, including the IPM PC-AT, to interface with interactive touch-based computer terminals that I designed for use in public information systems. I continued designing and developing related technology as a consultant to the Carroll Touch division of AMP, Inc., where in 1986 I designed one of the first custom touch-screen integrated circuits. I designed the touch/pen input system for the Linus WriteTop, which many believe to be the first commercial tablet computer.

7. From 1986 through 1987, I designed and built a high-performance computer system as a student at Carnegie Mellon University. From 1986 through early 1988, I also developed the curriculum, and supervised the teaching laboratory, for processor design courses.

8. In the latter part of 1989, I worked as a senior design engineer for ESL-TRW Advanced Technology Division. While at ESL-TRW, I designed and built a bus interface and memory controller for a workstation-based computer system, and also worked on the design of a multiprocessor system.

9. At the end of 1989, I (along with some partners) reacquired the rights to the technology I had developed at Touch Technology and at AMP, and founded The Graphics Technology Company. Over the next seven years, as an officer and a consultant for The Graphics Technology Company, I managed the company's engineering development activities and personally developed dozens of touch screen sensors, controllers, and interactive touch-based computer systems.

10. I have consulted, formally and informally, for a number of fabless semiconductor companies. In particular, I have served on the technology advisory boards for two processor design companies: BOPS, Inc., where I chaired the board, and Siroyan Ltd., where I served in a similar role for three networking chip companies – Intellon, Inc., Comsilica, Inc., and Entridia, Inc. – and one 3D game accelerator company, Ageria, Inc.

11. I have also served as a technology advisor to Motorola and to several venture capital funds in the U.S. and Europe. Currently, I am a director at Turtle Beach Corporation, providing guidance in its development of premium audio peripheral devices for a variety of commercial electronic products.

12. From 1991 through 1997, I served on the Faculty of Princeton University as an Assistant Professor of Electrical Engineering. At Princeton, I taught undergraduate and graduate-level courses in Computer Architecture, Advanced Computer Architecture, Display Technology, and Microprocessor Systems, and conducted sponsored research in the area of computer systems and related topics. From 1999 through 2002, I taught a Computer Architecture course to both undergraduate and graduate students at Stanford University multiple times as a Consulting Professor. At Princeton, I received several teaching awards, both from students and from the School of Engineering. I have also taught advanced microprocessor architecture to industry professionals in IEEE and ACM sponsored seminars. I am currently a lecturer at Santa Clara University teaching courses on Microprocessor Systems, Advanced Logic Design, Real-Time Computing, and Mechatronics. I teach about memory, including DDR SDRAM, in several of my classes and rely on the JEDEC specifications as industry standards.

13. From 1997 through 2002, I held a variety of executive positions at a publicly held fabless semiconductor company originally called S3, Inc. and later

called Sonicblue Inc. I held the positions of Chief Technology Officer, Vice President of System Integration Products, Senior Vice President of Business Development, and Director of Technology, among others.

14. In the roles listed above, I worked with and managed architecture and design teams responsible for the development of SRAM and DRAM memories, graphics chip memory controllers, and CPU memory controllers. I also worked with memory vendors and memory standards bodies, directly and through my staff, on the development of memory technology and standards. I have been involved with interpreting and understanding JEDEC memory standards since at least 1997. For many years, I had a direct-report staff member who would attend JEDEC meetings and bring me both proposed and final standards for review and comment. I also have used proposed and final JEDEC standards for chips, modules, and protocols to guide product decisions and to facilitate technical discussions with corporate partners and with consulting clients. I supervised design teams that implemented memory controllers for successful commercial products that interoperated with JEDEC-compliant DDR memory chips and memory modules.

15. My teams also developed the Rio MP3 players and a music delivery platform and webstore backend service for selling music. In 1999, this music delivery system was spun out as a separate company called RioPort.com. I served on the RioPort.com board of directors and became involved in their product and

technology strategy. I also managed engineering and marketing for the Rio product line for a period of time as an interim general manager. During my time at SonicBlue we launched more than 30 new consumer electronics products.

16. I served as a board member and technical advisor as KBGear Inc. from 1999-2001. KBGear Inc. designed and produced digital cameras and music players.

17. I have published more than fifty peer-reviewed papers in computer architecture and computer systems and IC design. I have also chaired IEEE and ACM conferences in microarchitecture and integrated circuit design and served as an associate editor for IEEE and ACM journals. I served on the IEEE Computer Society Awards committee. I am an IEEE Fellow and a Member of ACM. I am a named inventor on at least fifty-seven U.S. patents and thirty-seven foreign patents.

18. I have been the invited keynote speaker at the ACM/IEEE International Symposium on Microarchitecture and at the International Conference on Multimedia. I have also been an invited speaker on various aspects of technology or the PC industry at numerous industry events including the Intel Developer's Forum, Microsoft Windows Hardware Engineering Conference, Microprocessor Forum, Embedded Systems Conference, Comdex, and Consumer Electronics Show as well as at the Harvard Business School and the University

Illinois Law School. I have been interviewed on subjects related to technology and the electronics industry by publications such as the Wall Street Journal, New York Times, LA Times, Time, Newsweek, Forbes, and Fortune as well as CNN, NPR, and the BBC. I have also spoken at dozens of universities including MIT, Stanford, University of Texas, Carnegie Mellon, UCLA, University of Michigan, Rice University, and Duke University.

C. Compensation and Prior Testimony

19. I am being compensated at a rate of $600.00 per hour for my study and testimony in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

20. My CV, attached as Exhibit 1004, lists all other cases in which, during the previous 4 years, I have testified as an expert at trial or by deposition.

D. Information Considered

21. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in the Exhibit List at the end of this declaration.

22. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents

and information in forming any necessary opinions — including documents that may not yet have been provided to me.

23. My analysis of the materials produced in this matter is ongoing and I will continue to review any new materials as it is provided. This declaration represents only those opinions I have formed to date.

II. LEGAL STANDARDS FOR PATENTABILITY

24. In expressing my opinions and considering the subject matter of the claims of the ’912 Patent, I am relying upon certain basic legal principles that have been explained to me.

25. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

26. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as “prior art” and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

27. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the ’912 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that “a preponderance of

the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

28. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims, after being construed in this manner, are then to be compared to the information in the prior art.

29. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

30. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art. In this declaration I focus on "obviousness." My understanding of the legal standard for "obviousness" is set forth below.

31. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

32. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the asserted claims of the ’912 Patent would have been considered obvious as of the priority date of the patent.

34. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

35. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

36. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; satisfying a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of "objective factors" suggesting the claimed inventions are not obvious, and reserve my right to address any such evidence if it is identified in the future.

37. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market

demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

38. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

39. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the "ordinary innovation" and experimentation that does no more than yield predictable results, which are inferences and creative steps that a person of ordinary skill in the art would employ.

40. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these

issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

41. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words "teaching, suggestion, and motivation." I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), where the Court rejected the previous requirement of a "teaching, suggestion, or motivation to combine" known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

42. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor as of the priority

date of the patent and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

43. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourage or lead away from the line of inquiry disclosed in the reference(s). A reference does not "teach away" from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (e.g., because it would not work or explicit statements saying the combination should not be made).

44. I understand that a person of ordinary skill is also a person of ordinary creativity.

45. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary

skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance, the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE '912 PATENT

A. Effective Filing Date of the '912 Patent

46. The application that resulted in the '912 Patent (EX1001) is U.S. Patent Application Serial No. 11/862,931, filed Sept. 27, 2007. *See* EX1002. The '912 Patent claims priority to U.S. Provisional Application No. 60/588,244, filed on July 15, 2004 (EX1005, "the '244 provisional"), U.S. Provisional Application No. 60/550,668, filed on March 5, 2004 (EX1006, "the '668 provisional"), and U.S. Provisional Application No. 60/575,595, filed on May 28, 2004 (EX1007, "the '595 provisional"). EX1001 at front page at (60). The '912 Patent also claims priority as a continuation application to application No. 11/173,175, filed July 1, 2005, now U.S. Patent No. 7,289,386 (the '386 patent)

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(EX1008), which is a continuation-in-part of application No. 11/075,395, filed March 7, 2005, now U.S. Patent No. 7,286,436 (the '436 patent) (EX1009). EX1001 at front page at (63).

47. I understand that in order for a given claim of the '912 Patent to be entitled to the benefit of the filing date of an earlier application, the disclosure of that application must include, among other things, an enabling written description for the full scope of that claim. I further understand that a continuation-in-part application is an application filed during the lifetime of an earlier nonprovisional application, repeating some substantial portion or all of the earlier nonprovisional application and adding matter not disclosed in the earlier nonprovisional application (or applications).

48. As discussed below, two of the three prior art references I have considered (Perego, EX1035, and Amidi, EX1036) were filed before the earliest provisional application for the '912 Patent, which was filed on March 5, 2004, and thus for those two prior art references it is my understanding that it should not matter whether or not claim 16 of the '912 Patent is entitled to the filing date of any of the earlier applications that the '912 Patent claims priority to. However, another reference I have considered, Ellsberry (EX1037) was filed June 1, 2005, and thus, for the Ellsberry reference to be considered as prior art, it is my understanding that it does matter whether or not claim 16 of the '912 Patent is

entitled to the filing date of any of the earlier applications that the '912 Patent claims priority to.

49. For the reasons discussed below in ¶¶189-195, it is my opinion that claim 16 of the '912 Patent (EX1001) is not entitled to a priority date before the July 1, 2005, continuation-in-part application that resulted in the '386 Patent (EX1008). Therefore, it is my opinion that Ellsberry (EX1037) is also prior art to claim 16 of the '912 Patent. In any event, the references in the first two Grounds that I have considered (Perego alone or in combination with Amidi) were prior art even before March 5, 2004. Accordingly, my analysis for those Grounds does not depend on which priority date applies to claim 16 of the '912 Patent.

B. Person of Ordinary Skill in the Art ("Skilled Artisan")

50. Based upon my experience in the field and the information I have reviewed for purposes of this proceeding, I believe a person of ordinary skill in the art in the field of the '912 Patent (which I would describe as memory module design) in 2004 or 2005 ("Skilled Artisan") would have been someone with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working the field. Such a person would have been familiar with various standards of the day including the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and

SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. Specifically, he or she would have been knowledgeable about the JEDEC DDR and DDR2 SDRAM standards used to standardize the functioning of memory devices, and the JEDEC 21-C standard used to specify different possibilities for the physical layout of memory devices on a module as well as different possibilities for density and organization of the memory devices to achieve a given memory capacity. He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs and more low-level circuits such as tri-state buffers, flip flops and registers.

51. I have attached as exhibits some of the JEDEC standards that in my opinion a Skilled Artisan would have been familiar with as discussed above, including:

- DDR SDRAM standard (JESD79) (June 2000). *See* EX1030, EX1031.
- DDR2 SDRAM standard (JESD79-2) (September 2003). *See* EX1029, EX1039.
- JEDEC 21-C design specification (JESD21-C) for DDR RDIMM memory modules (January 2002). *See* EX1032, EX1040.

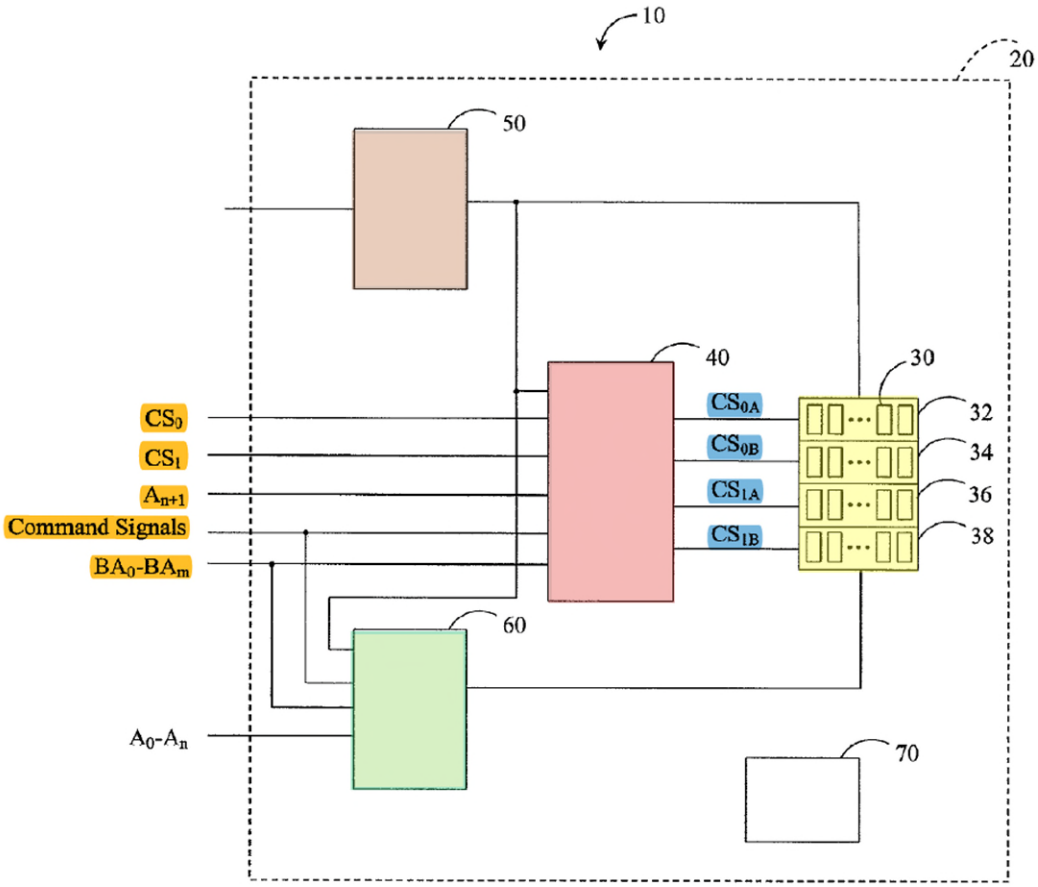
52. JEDEC's standards were and still are widely known and adhered to by those in the business of creating memory devices and modules. *See, e.g.*, EX1039, ¶ 4. In fact, the '912 Patent incorporates by reference one of the JEDEC standards to illustrate possible configurations of memory devices, and refers to standardized DDR2 memories and RDIMM memory modules. EX1001 at 12:28,12:34,12:39-43.

C. Overview of the '912 Patent (EX1001)

53. As illustrated in the annotated Figure 1A below, the '912 Patent (EX1001) discloses a memory module (10) that includes on a printed circuit board (20) a "first number" of memory devices (30, yellow), a logic element (40, red), a phase-lock loop device (50, brown), and a register (60, green). EX1001 at 5:6-45, FIG. 1A (reproduced below, annotated). The logic element (40, red) receives from a system memory controller (not shown) a set of input control signals (orange), including two chip select signals (CS_0, CS_1), a (row/column) address signal (A_{n+1}), Command Signals, and bank address signals (BA_0-BA_m). *Id*., *see also id*. at 6:55-63. The set of input control signals from the system memory controller corresponds to a "second number" of memory devices that is smaller than the "first number" of memory devices (yellow) on the module. *Id*. at 6:64-7:19. The logic element (40, red) generates a set of output signals (blue), including four chip select signals (CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}), that corresponds to the "first number" of

memory devices (yellow) on the module. *Id.* at 7:35-8:64. As shown in Fig. 1A, while the logic element 40 receives only two chip select signals corresponding to two ranks, the "first number" of memory devices (yellow) on the module are organized into four ranks 32, 34, 36, 38, each receiving a respective one of the four chip select signals (blue) generated by the logic element (40, red). *Id.* at 6:31-34, 7:20-29, 7:35-39, 7:55-8:64.

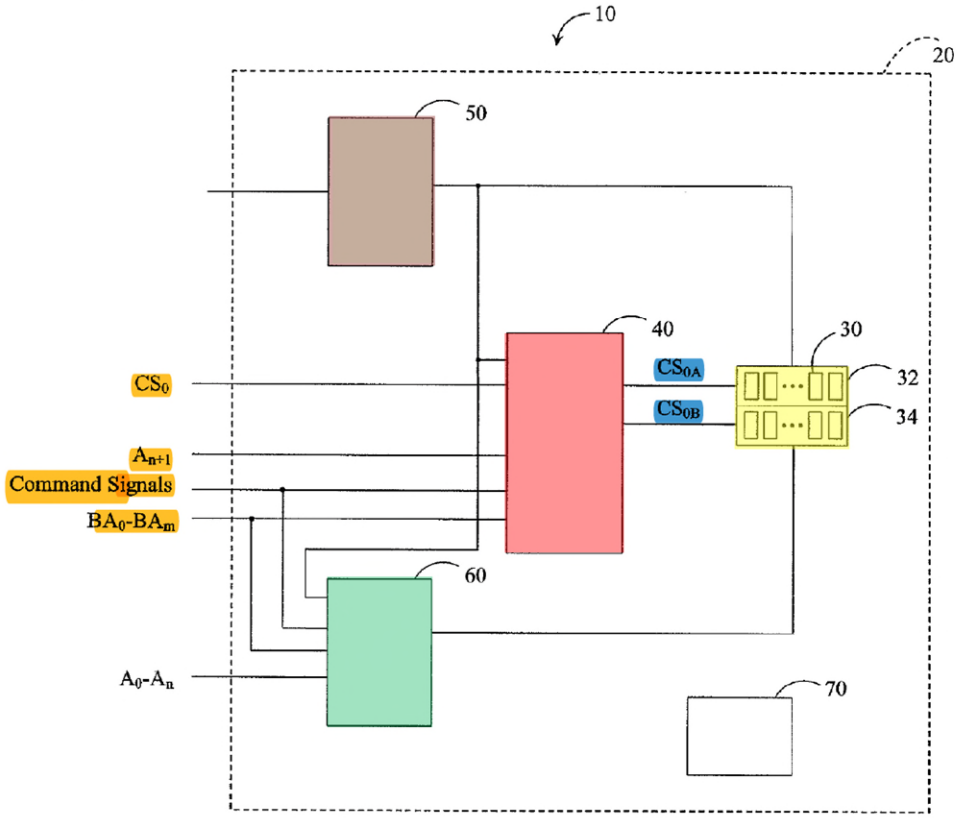
Figure 1A:



The '912 Patent discloses that the register (60, green) is separate from the logic element (40, red) and receives and buffers the remaining address signals A_0-A_n, as

well as the Command and bank address signals BA_0-BA_m, and transmits the registered signals to the memory devices (30, yellow). EX1001 at 5:22-45, Fig. 1A. The '912 Patent also discloses alternative implementations, including a module that receives only a single chip select signal (CS_0, orange, below) corresponding to a single rank ("second number of ranks") and a logic element (40, red) that generates two chip select signals (CS_{0A} and CS_{0B}, blue, below) corresponding to two ranks of memory devices on the module ("first number of ranks"). *Id*. at 7:3-9 ("For example, in the exemplary embodiment as schematically illustrated by FIG. 1A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of FIG. 1B, the first number of ranks is two while the second number of ranks is one.") & Fig. 1B (reproduced below, annotated).

Figure 1B:



54. In particular, the ’912 Patent discloses that, in the related art, “[m]emory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.” EX1001 at 1:31-34. The ’912 Patent further explains that “the ranks of a memory module are selected or activated by control signals” and that the control signals can include “rank-select signals, also called chip-select signals.” *Id.* at 2:35-39. Chip-select signals are standard signals in the JEDEC standards for DDR (sometimes called DDR-1) and DDR-2 memory devices, *see supra* ¶ 51, *infra* ¶¶73-76, which the ’912 Patent specifically indicates are

examples of memory devices compatible with the invention of the '912 Patent, EX1001 at 6:12-16, 22:5-14.

55. The '912 Patent seeks to improve the capacity of a memory module. EX1001 at 32:26-38. The '912 Patent's memory module appears to the computer system as if it had higher density memory devices (a system memory domain), while the physical configuration of the module (a physical memory domain) is different from what the computer system sees. *Id.* at 6:64-7:19. In the example shown in FIG. 1A (reproduced above), the memory controller issues commands to a module with two "virtual" ranks using two chip select signals (CS_0, CS_1), while the module actually has four ranks (32, 34, 36, 38, yellow), each having its own chip select signals (CS0A, CS0B, CS1A, CS1B). *Id.* at 6:31-34, 7:20-29, 7:35-39, 7:55-8:64.

56. The '912 Patent also discloses a logic table for rank selection based on an address signal A_{n+1} and chip select signals CS_0 and CS_1. EX1001 at 7:55-8:43. The '912 Patent also discloses that "[i]n certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time." EX1001 at 8:47-54.

57. The ’912 Patent also teaches that, when two memory devices form a single “virtual” memory device of higher capacity, like in the ’912 Patent, “collisions” may happen “between back-to-back adjacent read commands which cross memory device boundaries,” because the memory controller is not aware of those device boundaries. EX1001 at 23:60-24:12 & FIG. 5; *see also infra* at ¶¶192-194. The ’912 Patent teaches preventing such collisions by selectively connecting the system data bus to only one of the ranks that form the “virtual” higher density memory device. *Id*. at 24:23-25 (“collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines 104 of the memory devices from one another”).

D. <u>The Prosecution History</u>

58. The original claims of the ’912 Patent issued without any official rejections during prosecution. *See* EX1002. The original application for the ’912 Patent contained 21 claims, EX1002 at 47-21, but additional claims were added by amendments. There was one examiner interview, *id.* at 494-97, and then the claims were allowed, *id.* at 503-515. By the time of issuance, there were 51 claims. *Id.* at 517-20.

59. After the ’912 Patent issued, however, all previously issued claims were either cancelled or amended in *inter partes* reexamination after a series of

decisions by the Board resulting in a certificate issued February 8, 2021. EX1010 at 7966-73; EX1011 (Board Decisions); EX1012 (Reexamination Certificate).

60. In particular, there were three *inter partes* reexamination proceedings, Nos. 95/000,578 (EX1010), 95/000,579, and 95/001,339, which were merged on February 28, 2011, before any office actions. EX1010 at 1363-1370.

61. Claim 16 originally depended from independent claim 15. EX1001 at 38. As a result of the reexamination proceedings, however, claim 16 was amended and rewritten as an independent claim. EX1010 at 3106-07; EX1001 at 43-44.

62. The primary reference during reexamination was Amidi (EX1036). *See, e.g.*, EX1010 at 1393-1406, 3844-45, 4704-05, 7014-16, 7708-09 (anticipation and obviousness rejections based on Amidi).

63. During reexamination, Netlist admitted that Amidi "is probably the closest reference to the claims of the '912 patent," EX1010 at 1502, but Netlist argued that Amidi fails to disclose or render obvious a "logic element" that uses "bank address signals" to generate "output control signals in response to input control signals, which include bank address signals," as required by all of the claims of the '912 Patent (including claim 16, both before and after the amendments during reexamination), *id.* at 1502-06, 1646-50. Netlist submitted a declaration by an expert who argued that the claim language "in response to" required use of the input signals, including the "bank address" signals:

> 12. I note that Requester 2 contends that "in response to" does not require use of the transmitted signal. (*See*, *e.g.*, March 2012 Comments of Requester 2 at 10 and 29-30.) According to Requester 2, a "component will perform an operation 'in response to' a signal if it receives a signal and then, subsequently performs the operation." (*Id.* at 29.) I agree with the Examiner at ¶ 33 that such an interpretation ignores the "in response to" claim language. Requester 2 also points to Table 4 of the '912 patent as illustrating "several embodiments in which the logic element receives bank address signals, but does not use them in any way." (*Id.* at 29-30.) This is incorrect. Table 4 shows the types of signals that can be used as a density transition bit for different DDR2 memory densities of Table 3B. It shows that address signals (*e.g.*, A13 and A14) and bank address signals (*e.g.*, BA2) can be used as density transition bits depending on the type of memory devices being used. However, for the embodiments that employ address signals as the density transition bit, bank address signals are still used to generate output signals. Example 2 at Cols. 17-19 of the '912 patent make this clear. The Verilog code shows that gated CAS signals (such as cas0 in the code) are generated based not only on an address bit (such as a13 in the code) but also the bank address signals (such as bnk0 and bnk1 in the code) and an input chip select signal (such as ~rs0N_R in the code).

EX1010 at 4003. On May 31, 2016, in a Decision on Appeal, the Board found that Amidi discloses both a "register" and a "logic element" that receive bank address signals, EX1010 at 7036-37, but the Board agreed with Netlist that Amidi does not disclose "the limitation of generating a CAS or chip-select signal in response to a bank address signal," *id.* at 7074; *see id.* at 7075-78 (similar). The Board agreed that "[i]f the bank signal is not used in any way to generate the output signals, the generation of output signals cannot be in response to the bank signal." *Id.* at 7078. However, the Board found various claims obvious in light of Amidi in combination with other references. *See, e.g., id.* at 7084-85, 7096, 7099-7104. In response, Netlist amended some claims (but ***not*** claim 16) on July 31, 2016, to explicitly

require "wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response to at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal." EX1010 at 7317, 7319. Netlist argued, "Amidi's CPLD 604 never receives bank address signals and hence Amidi's control signals cannot be generated based on bank address signals. . . . Amidi does not use bank address signals to generate control signals (and certainly not the bank address signals and the at least one row address signal.)" *Id.* at 7320-21. In response, the Board agreed with Netlist that Amidi in combination with other references did not render obvious "the 'logic element' limitation, which claims the logic element generates chip-select signals in response to all four enumerated signals (i)-(iv) in claim 1." *Id.* at 7712-13; *see also id.* at 7719-20, 7720-21, 7723-24, 7726-27, 7733-34, 7737. The Board denied a request for rehearing and allowed the claims as amended. *Id.* at 7865-75. The Federal Circuit affirmed without an opinion. *Id.* at 7933.

64. In addition, throughout the reexamination Netlist argued that Amidi fails to disclose or render obvious a PLL "operatively coupled" to the "logic element" as required by all of the claims of the '912 Patent (including claim 16, both before and after the amendments during reexamination). EX1010 at 1506-10, 1656-60. Netlist argued during the reexamination that the construction of

"operatively coupled" should be narrowed to require that "the operations of the logic element 40 are clocked either directly or indirectly (e.g., through a clock buffer) by the output of the PLL 50" and that "the output of the PLL 50 controls the operation of the logic element 40." *Id.* at 1506. Netlist later amended some claims (but ***not*** claim 16) on July 31, 2016, to explicitly require "the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register." EX1010 at 7316, 7319. Netlist argued, "Amidi transmits a PLL clock signal to the register and memory, but not to the CPLD. Thus, Amidi does not disclose the PLL device transmitting the PLL clock to the *logic element*; the output of PLL 606 is neither directly nor indirectly transmitted to the CPLD 604." *Id.* at 7319-20. In response, the Board agreed with Netlist that Amidi in combination with other references did not render obvious this "logic element" limitation requiring the logic to generate certain signals in response to the PLL clock signal (as well as other signals). *Id.* at 7710, 7712-13, 7719-20, 7720-21, 7723-24, 7726-27, 7733-34, 7737. The Board denied a request for rehearing and allowed the claims as amended. *Id.* at 7865-75. The Federal Circuit affirmed without an opinion. *Id.* at 7933.

65. With respect to claim 16, in the Decision on Appeal on May 31, 2016, the Board agreed that Amidi did not disclose the last limitation of claim 16 requiring "the command signal is transmitted to only one DDR memory device at a

time." EX1010 at 7078-80. In particular, the Board agreed with the Examiner that "Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal *to only one DDR memory device at a time when there is a plurality of memory devices in a rank*. . . . Amidi's Figures 6A and 6B . . . teach or suggest that the command signal is transmitted to a cell within *multiple* memory devices at a time." EX1010 at 7079; *see also id.* at 7742. Netlist did not further amend claim 16 on July 31, 2016, as it did with the other claims discussed above to overcome various rejections in the Decision on May 31, 2016. *See* EX1010 at 7279-80, 7315-18, 7321.

66. The reexamination certificate reflecting all of the amendments to the claims of the '912 Patent discussed above issued on February 8, 2021. EX1012.

67. It is my understanding that within the family of the '912 Patent, many other claims have also been deemed invalid in various proceedings. For example, all claims in the '386 patent (EX1008) were cancelled during *inter partes* reexamination when the Board affirmed the Examiner's reexamination decision to cancel the claims on February 25, 2015 (EX1013) and a certificate was issued on August 19, 2016 (EX1014). These claims were directed to a memory module comprising "a logic element coupled to the printed circuit board, the logic element receiving a set of input control signals form the computer system, the set of input control signals corresponding to a second number of memory devices smaller than

the first number of memory devices" among other elements. EX1008. Likewise, all claims of U.S. Patent No. 7,636,274 (the '274 patent) (EX1015) were cancelled in *inter partes* reexamination after the Board's decision on May 9, 2017 (EX1016) resulting in a certificate issued November 5, 2018 (EX1017). Many other claims in this patent family have been found invalid in *inter partes* review (IPR) proceedings. For example, claims 15-17, 22, 24, 26, and 31-33 of U.S. Patent No. 7,881,150 (the '150 patent) (EX1018) were found to be unpatentable (EX1019, EX1020). Claims 1, 16, 17, 24, 30, and 31 of U.S. Patent No. 8,081,536 (the '536 patent) (EX1021) were found to be unpatentable (EX1022, EX1023). Claims 1-4, 6, 7, 10, 13, 17, and 23 of U.S. Patent No. 8,756,364 (the '364 patent) (EX1024) were found to be unpatentable (EX1025). And all claims of the '537 patent (EX1026) were found to be unpatentable (EX1027, EX1028).

68. In short, the prosecution history of the '912 Patent and of other patents in the same family show that Netlist has repeatedly drafted overbroad claims that have been allowed by the Examiner but subsequently have been determined to be invalid. In my opinion, claim 16 of the '912 Patent (even as amended during reexamination) is another example of such an overbroad, invalid claim, as discussed below.

E. Challenged Claims

69. This declaration relates to claim 16 of the ’912 Patent as amended during reexamination, which reads as follows:

Ref. #	Listing of Challenged Claims
[16.pre]	A memory module connectable to a computer system, the memory module comprising:
[16.a]	a printed circuit board;
[16.b]	a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,
[16.b.i]	the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
[16.c]	a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,
[16.c.i]	the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,
[16.c.ii]	the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,
[16.c.iii]	the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,

Ref. #	Listing of Challenged Claims
[16.c.iv]	wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and
[16.d]	a phase-lock loop device coupled to the printed circuit board,
[16.d.i]	the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
[16.e]	wherein the command signal is transmitted to only one DDR memory device at a time.

F. Construction of Terms Used in the '912 Patent Claims

70. I understand that in an *inter partes* review proceeding the claims of the patent are to be given ordinary and customary meaning in view of the specification and file history (i.e, the meaning that the term in question would have to a person of ordinary skill in the art at the time of the invention).

71. I also understand that where a patent applicant provides an explicit definition of a claim term in the specification that definition may control the interpretation of that term in the claim.

72. I also understand that if no explicit definition is given to a term in the patent specification the claim terms must be evaluated using the ordinary meaning of the words being used in those claims, evaluated from the perspective of a person of ordinary skill in the art.

1. "rank" and "chip select signal"

73. The '912 Patent states, "DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width." EX1001 at 2:16-18. "During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals." *Id.* at 2:35-39.

74. In my opinion, a Skilled Artisan would have understood that the term "rank" refers to an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module.

75. My opinion is consistent with the '912 Patent's use of the terms "rank" and "chip-select," quoted above, as well as how a Skilled Artisan would have understood the plain and ordinary meaning of the terms "rank" and "chip-select signal." *See, e.g.*, EX1033 (Memory Systems textbook) at 413 ("Essentially, a *rank* of memory is a '*bank*' of one or more DRAM devices that operate in lockstep in response to a given command," emphases in original); EX1029 (JESD79-2) at 6 ("Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code."); EX1032 (JESD21-C) at 4.20.4-10

through -16 (showing modules with one or two ranks, each rank receiving a respective chip select signal and having the full bit-width of the memory module).

76. I note that, at the time of the '912 Patent, the terms "physical bank" and "bank" were more general terms that, depending on the context, could be used to refer to what is now more typically described as a "rank." For example, the term "bank" was used not only to refer to a memory array *within* a single memory device, but also to one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module. Indeed, while the JESD79-2 standard dated September 2003 explained that a chip-select signal selects a "rank" as quoted above, the JESD79 standard originally published in June 2000 — which was still in use as of 2005 — used the term "bank" to mean exactly the same thing. *See* EX1030 (JESD79) at 7 ("Chip Select: All commands are masked when $\overline{S}$ is registered high. $\overline{S}$ provides for external bank selection on systems with multiple banks. $\overline{S}$ is considered part of the command code."). Similarly, the JESD21-C standard in 2002 used the term "physical bank" to refer to what is now more typically described as a "rank." *See*, *e.g.*, EX1032 (JESD21-C) at 6 (describing "S0-S3 SDRAM chip select lines" to select "Physical banks 0, 1, 2, and 3"), 10-16 (describing modules with one or two "physical banks" with a bit-width of 64 or 72 bits, each "physical bank" having a respective set of memory devices activated by

a corresponding (registered) chip select signal RS0 or RS1). Similarly, in previous Final Written Decisions invalidating claims in the same family as the '912 Patent, the Board has agreed that the "banks" in various prior art references correspond to the "ranks" claimed by Netlist. *See, e.g.*, EX1023 at 13–14, 20, 28 (Final Written Decision invalidating claims of U.S. Patent No. 8,081,536, EX1021). Over time, the term "rank" became preferred over the more general term "bank," as explained by the following textbook on memory systems, but at the time of the '912 Patent a Skilled Artisan would have understood that "bank" and "physical bank" could be used to mean the same thing as "rank" (given the "chip-select signal"):

10.2.2 Rank

Figure 10.5 shows a memory system populated with 2 ranks of DRAM devices. Essentially, a *rank* of memory is a *"bank"* of one or more DRAM devices that operate in lockstep in response to a given command. However, the word *bank* has already been used to describe the number of independent DRAM arrays within a DRAM device. To lessen the confusion associated with overloading the nomenclature, the word *rank* is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory system.

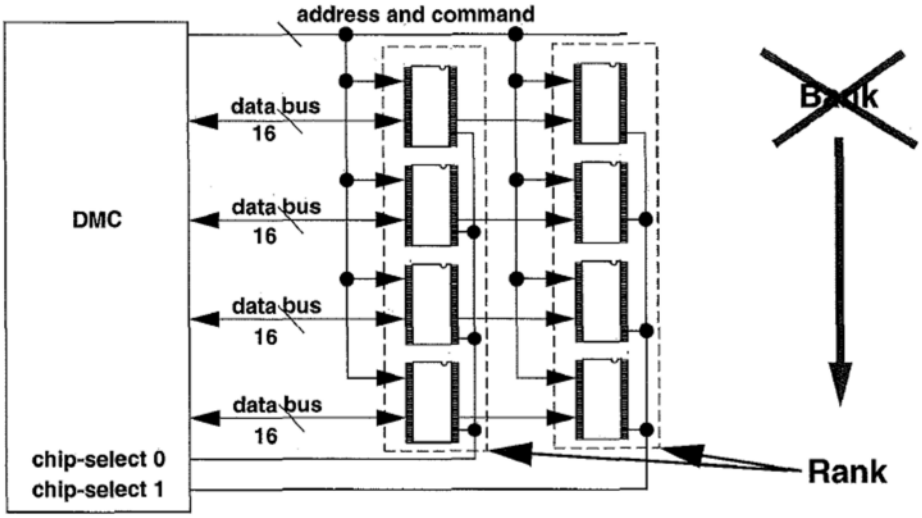


FIGURE 10.5: Memory system with 2 ranks of DRAM devices.

EX1033 at 413; *see also* EX1034 at 4n.3 (distinguishing between "rank" and a "bank" within a single DRAM), 9 ("Chip-select is used to enable ranks of DRAMs and thereby allow them to read commands off the bus and read/write data off/onto the bus.").

77. As discussed above, a "rank" can be formed by "one or more DRAM devices." EX1033 (Memory Systems textbook) at 413. For example, the '912

Patent describes an embodiment of a "rank" with one memory device: "[i]n certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices . . . ." EX1001 at 8:50-58. A Skilled Artisan would have understood from this disclosure that, "[i]n such embodiments," each rank has only one memory device, because "the command signal[, e.g., read,] is passed to the selected rank only," and this command signal "is sent to only one memory device." In this embodiment, where there is only one memory device in the "rank," the bit width of the "rank" would be the same as the bit width of the memory device, for example 16 bits. The '912 Patent explains that "memory devices . . . having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein." *Id.* at 6:16-:19.

IV. OVERVIEW OF THE PRIOR ART

A. U.S. Patent No. 7,363,422 to Perego (EX1035)

78. United States Patent No. 7,363,422 to Perego ("Perego") was filed January 28, 2004, published on September 23, 2004, and issued as a patent on

April 22, 2008. EX1035. I therefore understand that Perego is prior art to the '912 Patent pursuant to at least 35 U.S.C. § 102(a) & (e), at least because of its filing date. Perego was not discussed during prosecution or reexamination of the '912 Patent and is not a reference cited in the '912 Patent. *See* EX1001, EX1002, EX1010.

79. Perego discloses a memory system, such as memory system 305, that includes a memory controller 310 connected to multiple buffered memory modules 330a-330c, such as memory module 340 (representing memory module 330a) that includes a buffer device (350, red) and multiple groups of memory devices (360, green and blue). EX1035, *e.g.*, at Abstract, 4:63-5:15 & Fig. 3B (reproduced below, annotated).

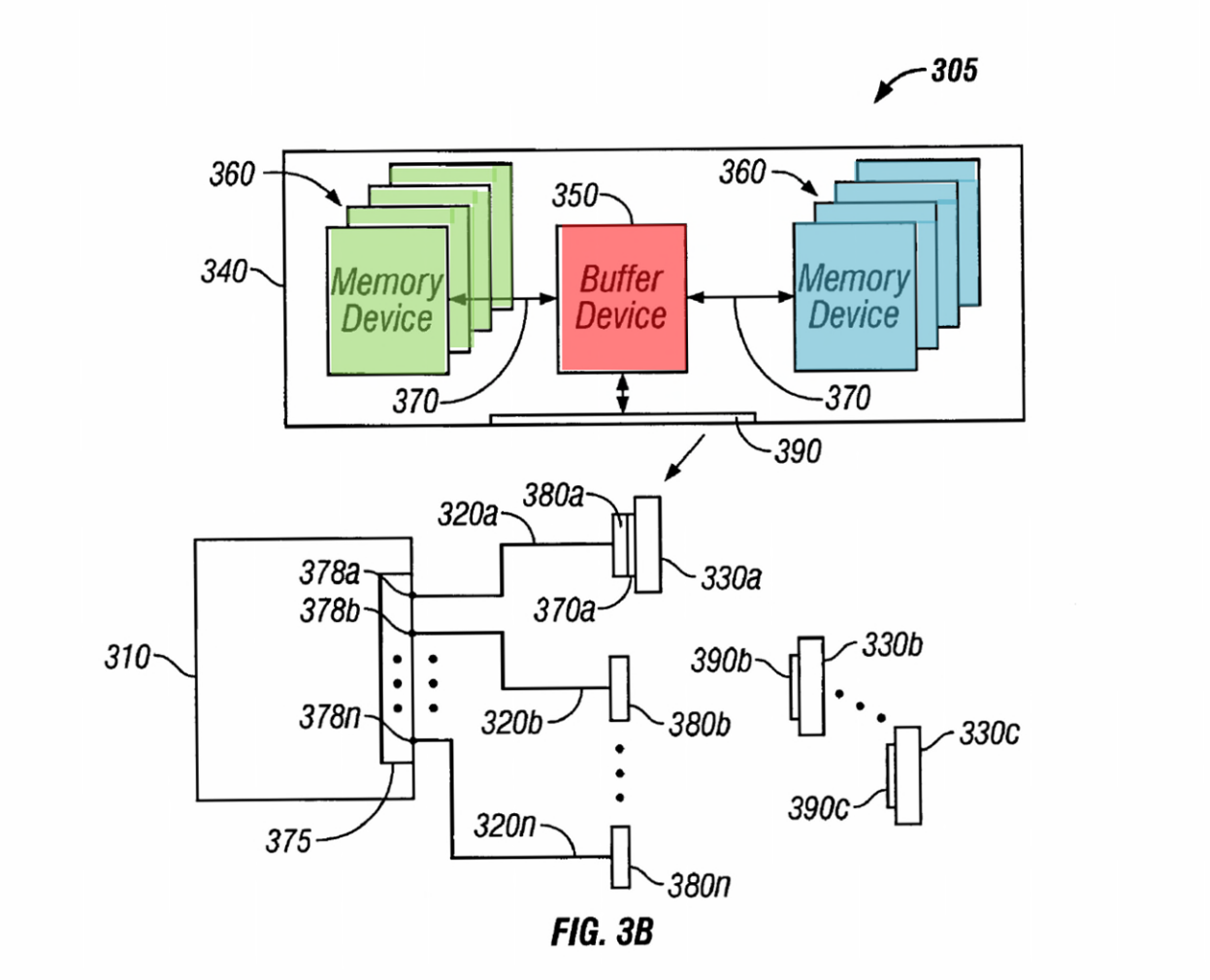


FIG. 3B

80. Furthermore, Perego's FIG. 3C shows an example of a buffered module 395 that includes a configurable width buffer device 391 (red) and memory devices 360 organized in groups (green, blue), and can be used in conjunction with the system described above. EX1035 at 7:30-34, Fig. 3C (reproduced below with annotations).

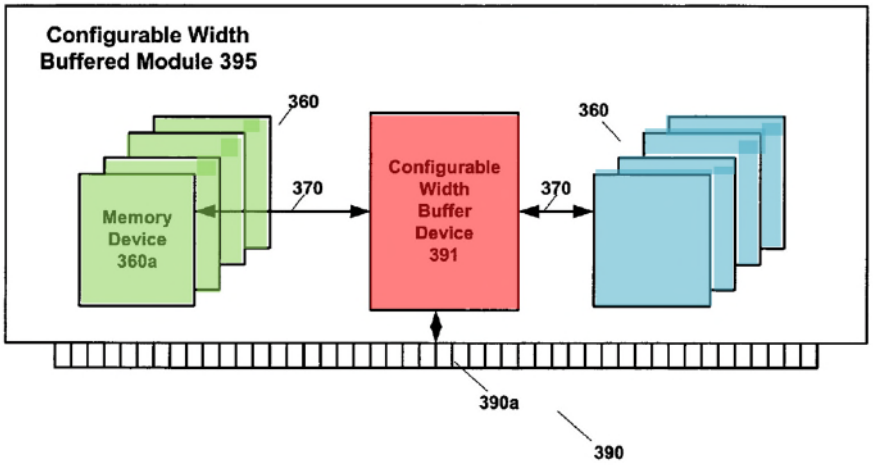


Fig. 3C

81. The purpose of Perego's invention was to fill the "need for memory system architectures or interconnect topologies that provide flexible and cost-effective upgrade capabilities while providing high bandwidth to keep pace with microprocessor operating frequencies." EX1035 at 2:26-29. Accordingly, Perego's "[b]uffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices." EX1035 at 6:34-43.

82. Perego's FIG. 5B illustrates an implementation of "a configurable width buffer device 391 as seen in FIG. 3C," shown above. EX1035 at 13:6-10,

FIG. 5B (reproduced below with annotations). For example, the buffer device 391 includes interfaces 520a and 520b that are programmable to accommodate different numbers and types of memory devices, and also includes a configurable width interface 590 to communicate with the memory controller. *Id*. at 13:60-14:15.

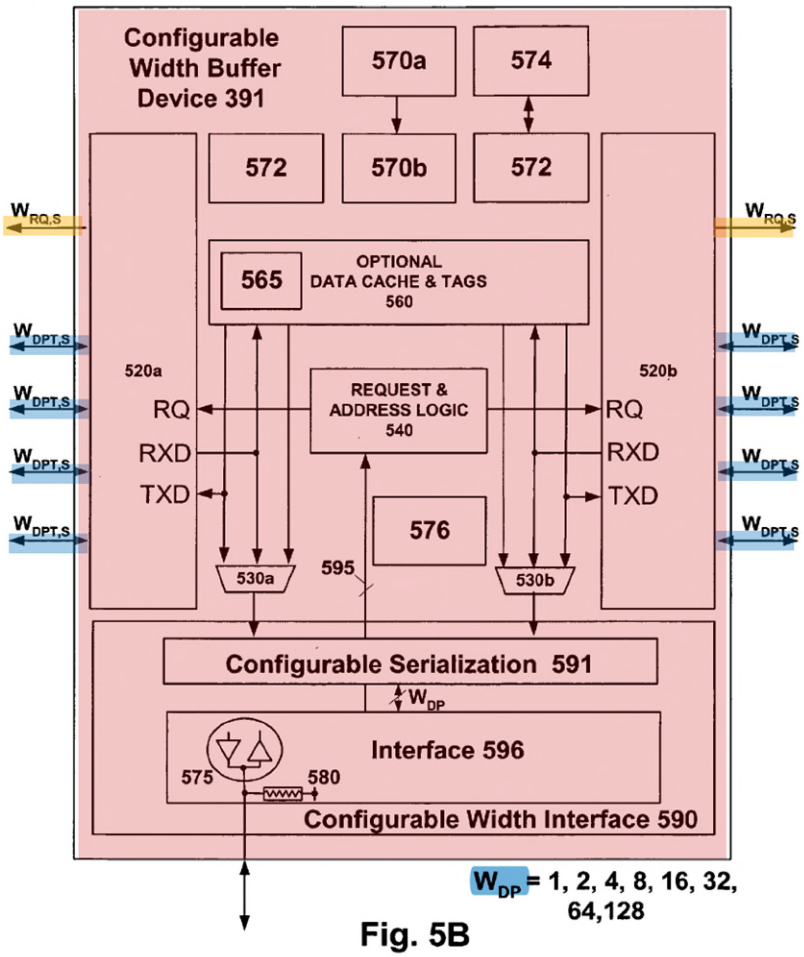


Fig. 5B

83. Perego also discloses an embodiment of the configurable width interface 590, which includes input and output latches 597f–m (blue), including

two latches for each data connection of the configurable width buffer device. EX1035 at FIG.5C (reproduced below with annotations), 17:22-26, 17:61-67.

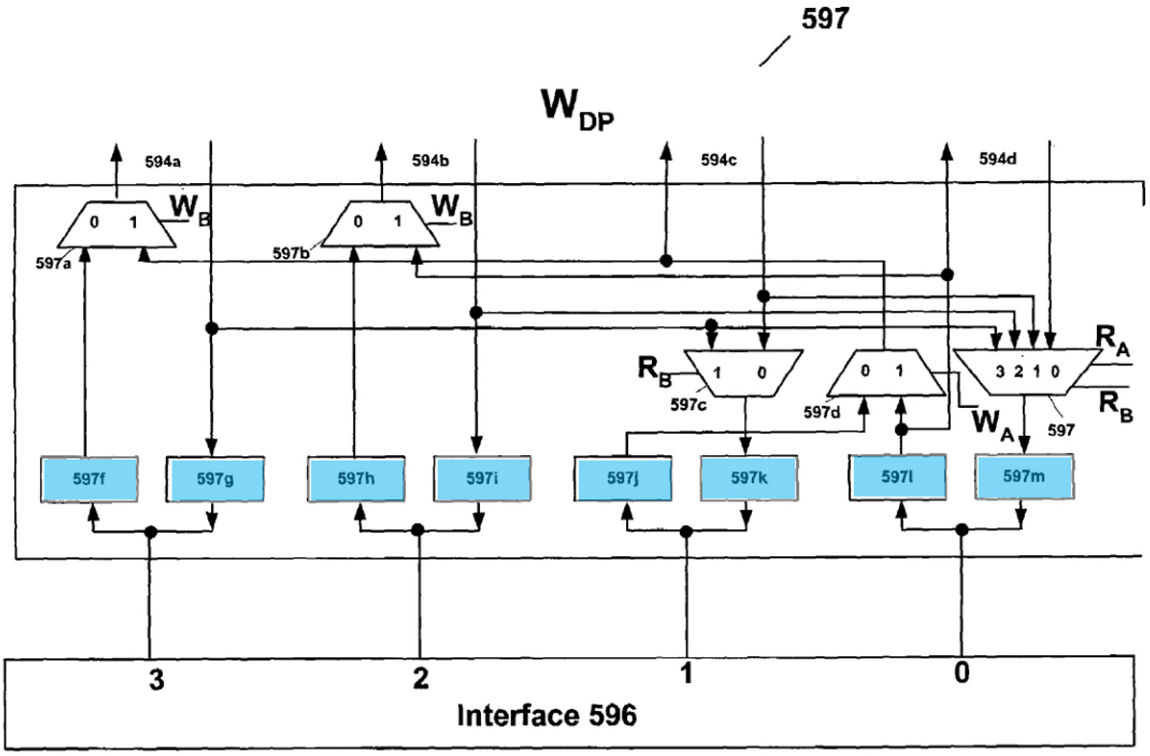


Fig. 5C

84. Perego further discloses that its buffer device includes a serial interface 574 and operations circuit 572 which may provide information to the memory controller that can be used, for example in initialization, to properly configure and operate the system, including module or memory device identification values, test function, set/reset, access latency values, vendor specific functions or calibration related information. EX1035 at 12:20-34; FIGS. 5A and 5B.

B. U.S. Patent Pub. No. 2006/0117152 to Amidi (EX1036)

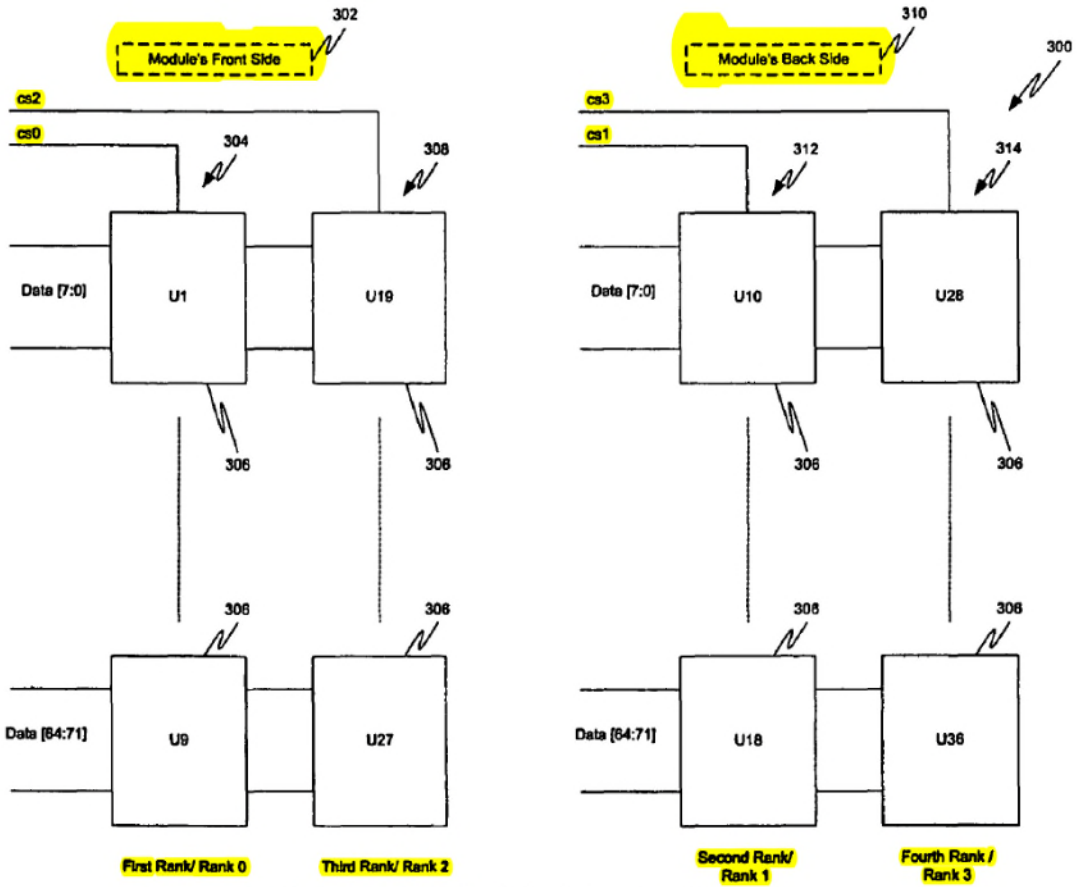
85. U.S. Patent Application Publication No. 2006/0117152 to Amidi et al. ("Amidi") was filed on January 5, 2004, and published on June 1, 2006. EX1036 at front page. I therefore understand Amidi to be prior art to the '912 Patent pursuant to at least 35 U.S.C. § 102(a) & (e), at least because of its filing date. Amidi was cited in the '912 Patent and discussed by the Board as a primary reference during reexamination, as discussed above in ¶¶ 59-66. Notably, it is my understanding that Netlist narrowed claims of the '912 Patent to distinguish them from what was taught by Amidi. *See id.* However, I note that Amidi was not considered in combination with Perego. *See id.*

86. Amidi discloses a four rank memory module for standard two rank sub-systems. EX1036 at Title. Amidi explains that prior-art memory modules typically had one or two ranks of memory devices, and were configured to be inserted into sockets on the computer's main board. EX1036 at [0002-0007]. "Common system implementations 100 have typically two memory chip selects routed per socket … [where t]he system chip select signals control individual memory modules ranks." *Id.* at [0003].

87. Amidi further explains that "[b]ecause memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices. However,

in order to achieve a [higher] density . . . the memory module needs four ranks." EX1036 at [0008]. "A need therefore exists for a transparent four rank memory module fitting into a memory socket having two chip select signals routed." *Id.* at [0011].

88. Amidi is directed to such a four-rank memory module. EX1036 at [0001]. Each rank of Amidi's memory module has a corresponding chip select signal as shown in Amidi's FIG. 3 (reproduced below with color annotations, showing four ranks of memory devices, namely Rank 0 and Rank 2 on the front, and Rank 1 and Rank 3 on the back, each rank receiving a respective chip select signal cs0, cs2, cs1, and cs3).



Transparent Four Rank DDR Module Block Diagram
FIG. 3

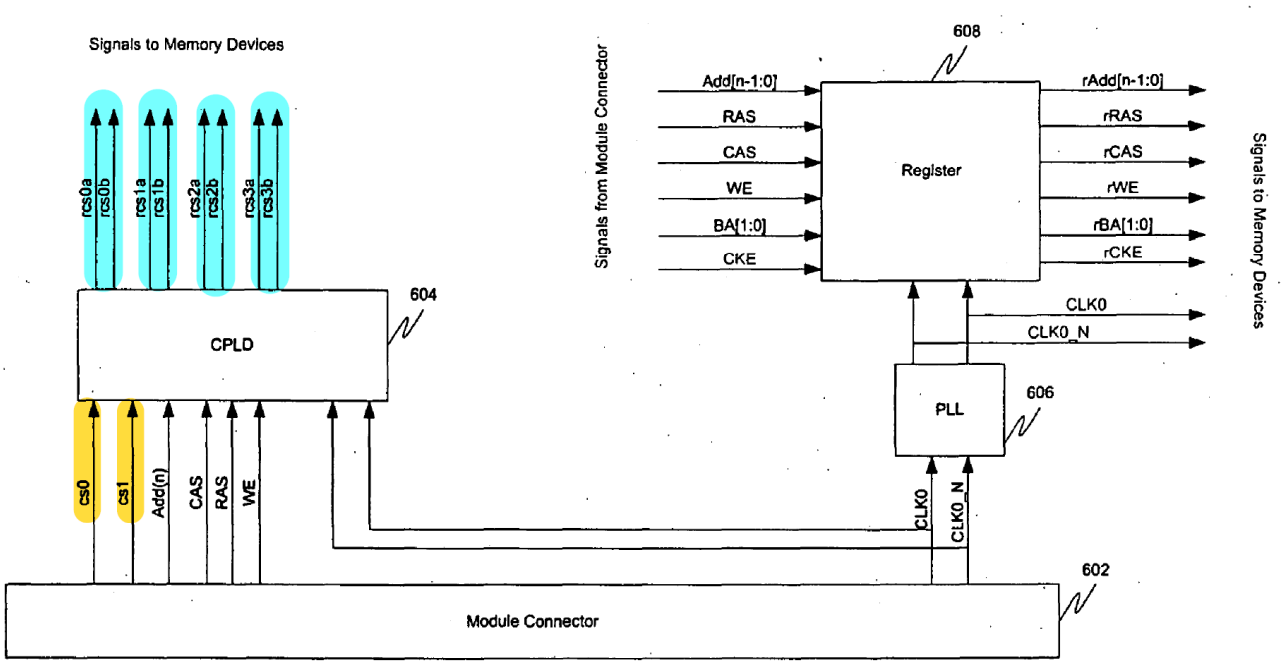
89. Amidi's memory module also includes a "[Complex Programmable Logic Device] CPLD 410 [which] emulates a two rank memory module on the four rank memory module 400. CPLD 410 allows a system having a memory socket with only two chip select signals routed to interface with a four rank memory module . . . . The CPLD 410 determines which rank from the four ranks to activate based upon the address and command signals from a memory controller coupled to the memory module 410." *See* EX1036 at [0041], FIG. 4A (CPLD 410).

90. For a read or write operation, Amidi's CPLD determines which of the four ranks is active based on the first and second chip select signals CS0 and CS1,

and the highest row address bit Add(n), as depicted in the table of FIG. 5 (below). EX1036 at FIG. 5, [0043].

Add(n)	CS1	CS0	Active Bank
0	1	0	0
0	0	1	1
1	1	0	2
1	0	1	3

91. Amidi's CPLD also "ensures that all commands for a two rank memory module conveyed by the module connector 602 are also performed on the four rank memory modules." *Id.* at [0052]. For example, when a load mode register command is issued, two ranks are activated. *Id.* (last two sentences). To activate these ranks properly for all commands, Amidi's CPLD uses command signals such as CAS, RAS, and WE in addition to the chip select signals cs0 and cs1 and the row address, and generates four chip select signals rcs0, rcs1, rcs2, and rcs3 (one for each rank) as shown in the detailed block diagrams of Amidi's FIG. 8 and FIG. 6A (the latter reproduced below with annotations highlighting the two received chip selects in orange and the generated four chip selects in light blue).



Row Address Decoding
FIG.6A

92. Amidi also emphasizes that "[m]any other families of memory devices or densities of memory devices (not shown) may be used to build the four rank memory module. Those of ordinary skill in the art will appreciate that the example of four rank memory module described above is not intended to be limiting and that other configuration can be used without departing from the inventive concepts herein disclosed." EX1036 at [0071].

C. U.S. Patent Pub. No. 2006/0277355 to Ellsberry (EX1037)

93. U.S. Patent Application Publication No. 2006/0277355 to Ellsberry ("Ellsberry") (EX1037) was filed on June 1, 2005 and published on December 7, 2006. I understand that Ellsberry is prior art to the '912 Patent pursuant to at least

35 U.S.C. § 102(a) & (e) assuming the '912 Patent is not entitled to a priority date earlier than July 1, 2005, which I believe to be the case, as discussed below, ¶¶189-195. During the original prosecution of the '912 Patent, Ellsberry was cited by the examiner as "pertinent" but was not considered because it was "filed after the ['912] application's earliest effective filing date." EX1002 at 510. In a Final Written Decision in an IPR against another patent owned by Netlist, the Board made numerous findings about what Ellsberry discloses. EX1038.

94. Ellsberry discloses that the "term 'memory module' refers to any package in which one or more memory devices are mounted (e.g., DIMM, SIMM, etc.)." EX1037 at [0023]. In Ellsberry's invention, a "control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch. By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system. That is, the invention expands the addressable memory banks on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device." EX1037 at Abstract. For example, Figure 12 illustrates a configuration of a memory module "that can be built using combinations of the control unit and bank switch according to various

embodiments of the invention." EX1037 at [0052], Fig. 12 (reproduced below, annotated).

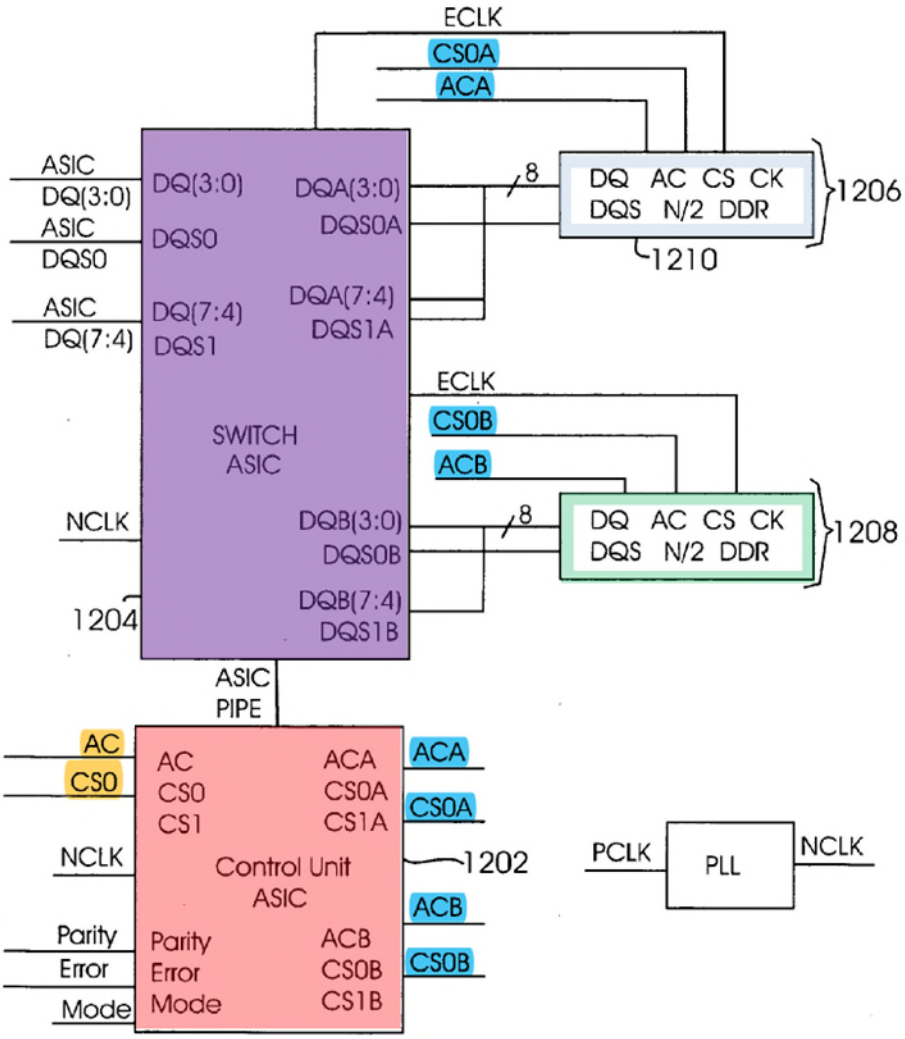


Fig. 12

In particular, "FIG. 12 illustrates a single chip-select memory configuration in which one control unit 1202 [(red)] and one bank switch 1204 [(purple)] are used to control two memory banks 1206 [(light blue frame)] & 1208[(light green frame)], each memory bank having one memory device 1210." EX1037 at [0055].

As also shown in Figure 12, the control unit (1202, red) receives a single chip select signal (CS0, orange) and corresponding address and command signals (AC, orange) to control a single memory rank and generates two chip select signals (CS0A and CS0B, blue) and address and command signals (ACA and ACB, blue) for two memory ranks.

V. COMPARISON OF THE PRIOR ART TO CLAIM 16 OF THE '912 PATENT

95. In my opinion, as discussed below, claim 16 of the '912 Patent, as amended during reexamination, is obvious in light of Perego alone (Ground 1) or in view of Amidi (Ground 2), and is also obvious in light of Ellsberry (Ground 3).

A. Grounds 1 and 2: Claim 16 Is Rendered Obvious by Perego Alone (Ground 1) or In View of Amidi (Ground 2)

1. Motivation to Combine Perego and Amidi (for Ground 2)

96. As discussed below in detail for Ground 1, Perego alone discloses or renders obvious to a Skilled Artisan the limitations of Claim 16 of the '912 Patent. However, to the extent one might argue that Perego alone does not sufficiently disclose or suggest those limitations, they would have been obvious in light of Amidi, as explained for Ground 2. For example, a Skilled Artisan would have been motivated to combine functionalities of the memory module of Amidi with the memory module described in Perego in order to achieve the advantages of rank multiplication as taught by Amidi.

97. Perego and Amidi are analogous art to the '912 Patent as each is directed to the same field of memory modules and tries to solve the problem of improving the performance and upgrade flexibility of memory modules. *See, e.g.*, EX1035 (Perego) at 3:13-28 ("The present invention relates to a memory system which includes one or more semiconductor memory devices coupled to a buffer device. The buffer device may be disposed on a memory module, housed in a common package along with memory devices … In several embodiments, the buffer device provides for flexible system configurations, and several performance benefits. For example, the buffer device may be a configurable width buffer device to provide upgrade flexibility and/or provide high bandwidth among a variety of possible module configurations in the system."); EX1036 (Amidi) at [0002] ("Computers use memory devices for the storage and retrieval of information. These memory devices are often mounted on a memory module to expand the memory capacity of a computer."), [0018] ("Because memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices."); EX1001 ('912 Patent) at 1:21-24 ("The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules."), 5:1-5 ("Thus, when the cost of a higher-density

DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.").

98. Accordingly, a Skilled Artisan would have been motivated to implement the rank multiplication functionality taught by Amidi in the memory module of Perego in order to lower the cost and to increase upgrade flexibility of the memory modules. EX1036 (Amidi) at [0018] ("Because memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices.").

99. For example, Perego discloses that its "[b]uffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices." EX1035, 6:34-43. Perego also discloses the importance of being "cost effective." *Id.* at 2:26-30.

100. Furthermore, both Perego and Amidi teach that the module can hide the type of memory devices it actually uses from the system memory controller and

pretend to have a different type of memory devices, providing a further motivation to combine the teachings of Perego and Amidi. EX.1035 (Perego) at 10:56-67 ("Utilizing buffer device 405 between the memory devices and controller in accordance with the present invention (e.g., see FIG. 3) may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation."), EX.1036 (Amidi) at [0011] ("A need therefore exists for a transparent four rank memory module fitting into a memory socket having two chip select signals routed.").

101. A Skilled Artisan would have understood from this disclosure that Perego's module can include memory devices of prior generations ("retaining backward compatibility with existing generations of memory devices") while interfacing with new generations of memory controllers designed to communicate with new generations of memory devices (or vice versa, using new generations of memories to upgrade older memory systems). For example, Amidi teaches that new generations of memory devices have higher capacity, but they are more expensive than existing memories of corresponding capacity, so older memories can be advantageously used to upgrade newer memory systems. Ex1036 (Amidi) at [0018] ("Because memory devices with lower densities are cheaper and more

readily available, it may be advantageous to build the above same density memory module using lower densities devices."). Therefore, a Skilled Artisan would have been motivated to use lower-capacity memory devices in memory systems configured for higher-capacity memory devices and advantageously lower the cost of the modules.

102. A Skilled Artisan would have also understood that the teachings of Perego and Amidi are not limited to different generations of memories or the corresponding price differences, because these references also disclose the advantages of design flexibility from designing a memory module with one type of memory devices and using that module in a system where the memory controller is designed for different type of memory devices. EX1035 (Perego) at 3:23-28 ("In several embodiments, the buffer device provides for flexible system configurations, and several performance benefits. For example, the buffer device may be a configurable width buffer device to provide upgrade flexibility and/or provide high bandwidth among a variety of possible module configurations in the system."); EX1036 (Amidi) at [0071] ("Many other families of memory devices or densities of memory devices (not shown) may be used to build the four rank memory module. Those of ordinary skill in the art will appreciate that the example of four rank memory module described above is not intended to be limiting and

that other configuration can be used without departing from the inventive concepts herein disclosed.").

103. Therefore, a Skilled Artisan would have been motivated to implement Perego's module with one type of memory devices, such as lower-capacity memory devices, and configure Perego's buffer to respond to control signals for another type of memory device, such as a higher-capacity memory device, as taught by Amidi, in order to upgrade a system configured to handle those higher-capacity memory devices.

104. The combination of Perego and Amidi would have been well within the level of skill, and provided nothing more than what was expected from such a combination. For example, both Perego and Amidi disclose to a Skilled Artisan how to make a module with one type of memory devices and add an interface that can communicate with a memory controller that is configured to control a different type of memory devices according to the relevant standards at the time. For example, a Skilled Artisan would have understood those standards at the time and the differences between the different standardized memory devices and their respective control signals. *See, e.g.*, EX1036 (Amidi) at [0004] ("Standard memory modules such as memory module 106 have either one rank or two rank of memory devices. Each memory device comes in a variety of configurations and families such as 128 Mbit, 256 Mbit, 512 Mbit, and 1024 Mbit DDR SDRAM

families. Each of these families is further divided into three distinct flavors such as x4, x8, and x16 data bits."), *see also id*. at [0047-49], [0055-57] (comparing exemplary memory devices and techniques to use one type of memory devices to emulate another type of memory devices); EX1029 (JESD79-2) at 7-8 (describing standard DDR2 memory devices and their corresponding addressing schemes).

105. Furthermore, a Skilled Artisan would have understood that the combination of Perego and Amidi can solve problems like back-to-back read operations across device boundaries. Indeed, Perego teaches that each memory device can have its own channel to interface with the buffer device. EX1035 (Perego) at 10:17-20 ("a dedicated channel between each memory device and the buffer device may be implemented on the module"). Perego also teaches that such dedicated channels and the corresponding interface include data strobe lines. *Id*. at 14:4-10 ("an additional complement data strobe signal for each byte of each memory device may be programmed at interfaces 520a and 520b to accommodate different types of memory devices on a configurable width memory module 395, such as legacy memory devices that require such a signal."). A Skilled Artisan would have understood that, by implementing dedicated channels and corresponding interfaces as disclosed by Perego, there are no conflicts on the data strobe lines of two different memory devices, because the different data strobe lines are connected to different interfaces. Indeed, Perego teaches to use input and

output latches to couple to data lines. *Id*. at 17:34-35 ("Multiplexer/demultiplexer circuit 597 includes four pairs of read and write data line pairs 594a–d coupled…"); Fig. 5D (showing input-output latches 597f-m coupled to data lines) and 18:65-66 ("In embodiments of the present invention, interfaces 520a and 520b include multiplexer/demultiplexer circuit 597 …"). A Skilled Artisan would have understood that read data is captured by such latches using the data strobe signals. Thus, by latching the read data separately for each memory device, there is no conflict between the data strobe signals of different devices.

106. Therefore, the combination of Perego and Amidi would have provided nothing more than what was expected at the time, a memory module that is built with one type of memory devices, e.g., lower-capacity memory devices, and operates in a system where the memory controller issues commands for another type of memory devices, such as higher-capacity memory devices.

2. Claim 16 is Unpatentable

a) [16.pre] A memory module connectable to a computer system, the memory module comprising:

107. To the extent the preamble is limiting, Perego discloses a "*memory module connectable to a computer system, the memory module comprising*."

108. For example, as shown below in Figure 3B, Perego discloses a memory module, such as memory module 340 (which is a more detailed

representation of memory module 330a), that is connectable to a computer system, such as memory system 305, including a controller 310 coupled to memory modules, such 330a, 330b and 330c through respective connectors 380a, 380b and 380c. EX1035 (Perego) at Fig. 3B (reproduced below, annotated). As illustrated in Figure 3B of Perego, memory module 340 includes a buffer device 350 (red) and memory devices 360 (green).

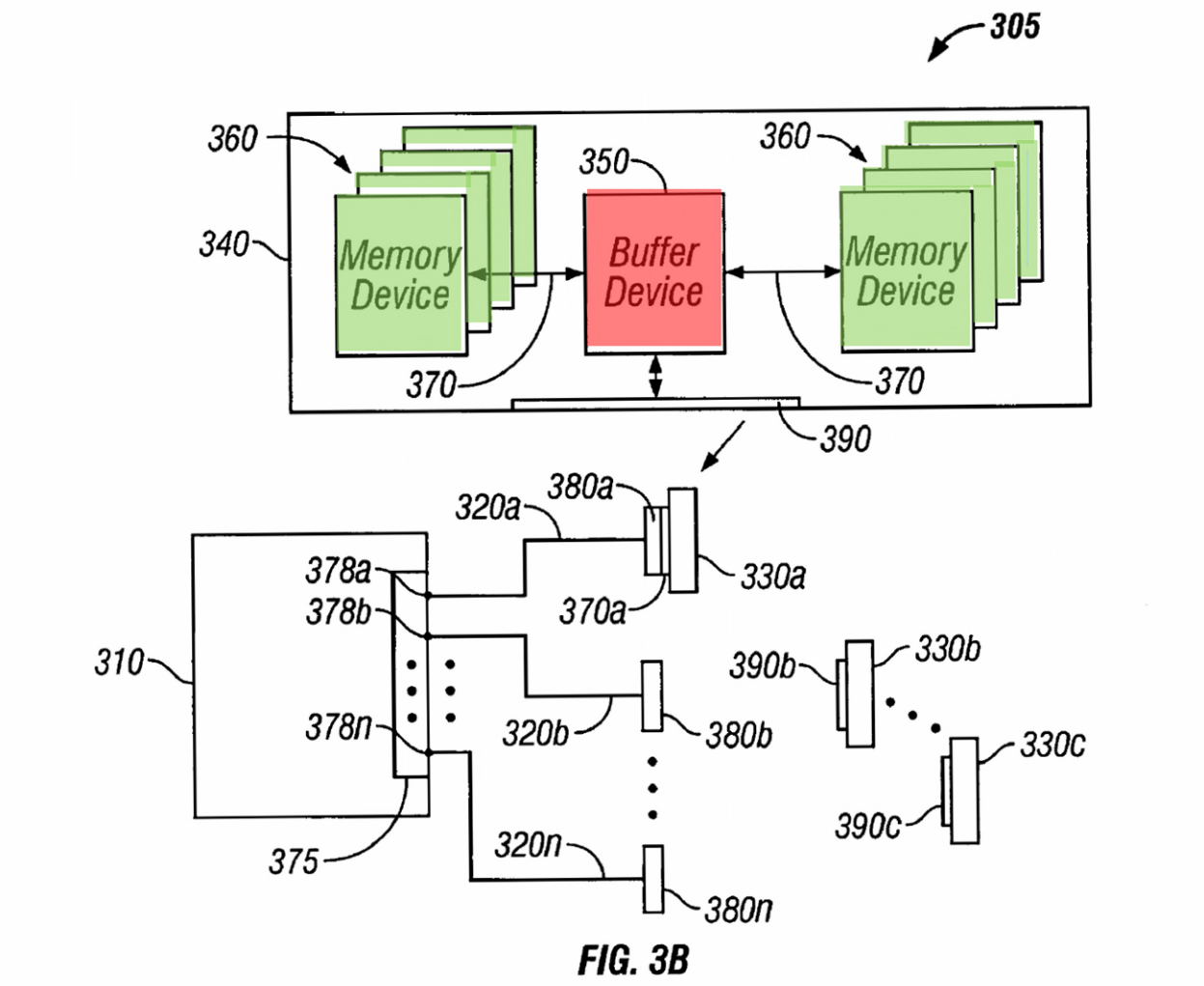


FIG. 3B

109. Perego discloses that the memory modules (also called "memory subsystems" in Perego) "are incorporated onto individual substrates (e.g.,

PCBs) … that include connectors 390a-390c … Corresponding mating connectors 380a–380n are connected to a connection point of each point-to-point link 320a–320n. Each of mating connectors 380a–380n interface with connectors 390a–390c to allow removal/inclusion of memory subsystems 330a–330c in memory system 305. In one embodiment, mating connectors 380a–380n are sockets and connectors 390a–390c are edge connectors disposed on an edge of each memory subsystems 330a–330c. Mating connectors 380a–380n, are attached to a common substrate shared with point-to-point links 320a–320n and controller 310." EX1035 (Perego) at 5:56-6:11. Perego also discloses that "interface connections 390a includes a plurality of contacts, conducting elements or pins." *Id*. at 7:39-41; *see also id*. at 4:19-22 ("A 'memory module' or simply just 'module' denotes a substrate package housing or structure having a plurality of memory devices employed with a connector interface.").

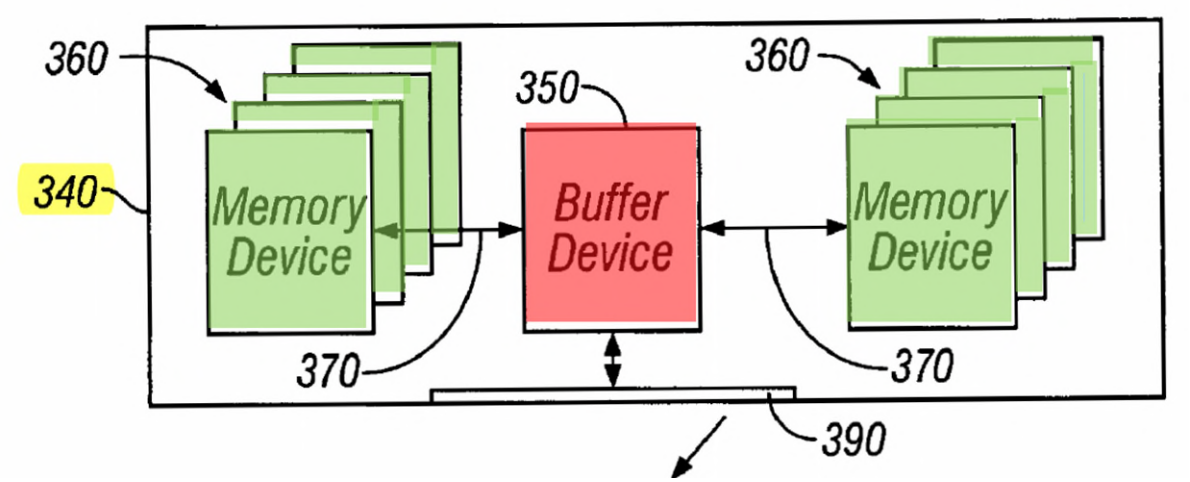
110. Thus, Perego discloses "*a memory module connectable to a computer system*" as recited by Claim 16.

b) *[16.a]* a printed circuit board

111. Perego discloses that its memory module includes "*a printed circuit board*."

112. For example, Perego discloses that the memory modules (also called "memory subsystems" such as memory subsystem 340, yellow) "are incorporated

onto individual substrates (e.g., PCBs)." EX1035 (Perego) at 5:60-62, Fig. 3B (reproduced below in part, annotated). PCB is the common acronym for "printed circuit board." *Id.* at 5:59-60.



113. Thus, Perego discloses that its module includes "*a printed circuit board*" as recited by Claim 16.

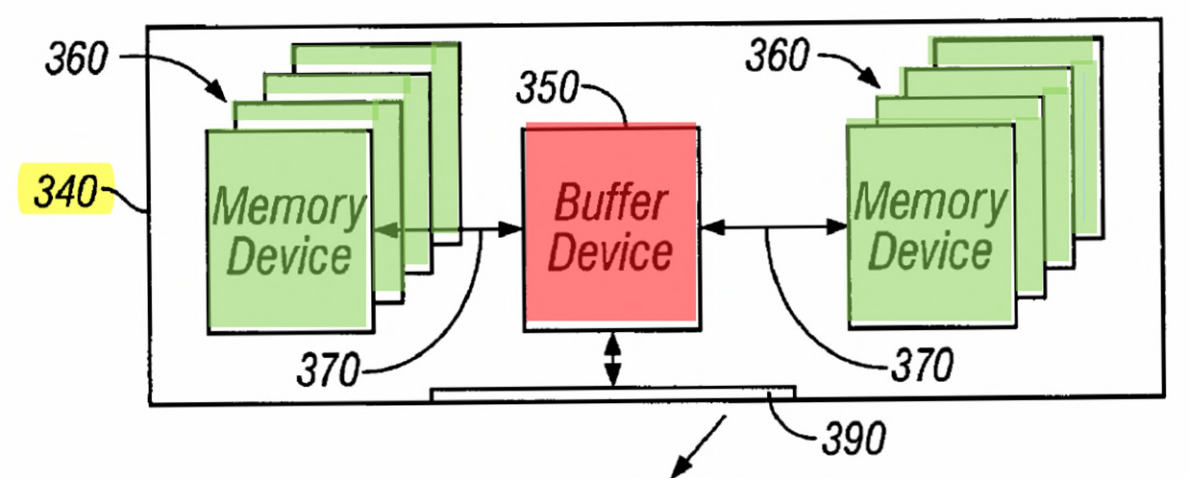
c) *[16.b]* a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,

114. Perego discloses that its memory module includes "*a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board*."

115. For example, Perego discloses that "memory devices 360 [(green)] are discretely packaged Synchronous type DRAM integrated circuits (ICs), for example, DDR memory devices, …" EX1035 (Perego) at 8:1-9 & Fig. 3B (reproduced above, annotated), *see also id.*, 3:62-4:3 (defining the term "Memory devices" and explaining that "[e]xamples of types of memory devices include

dynamic random access memory (DRAM), static random access memory (SRAM), and double data rate SDRAM (DDR).”), 10:56-59 (“memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices.”).

116. Perego also discloses that these memory devices are coupled to the printed circuit board. As discussed above with reference to claim element **[16.a], ¶¶111-113**, memory subsystems, such as memory subsystem 340 “are incorporated onto individual substrates (e.g., PCBs [printed circuit boards]),” EX1035 (Perego) at 5:60-62, 5:59-60, and “a plurality of memory devices 360 are disposed on memory subsystem 340,” *id*. 5:3-4. Perego further discloses that a “[b]uffer device 350 [(red)] is coupled to the plurality of memory devices 360 [(green)] via channels 370.” *Id*. at 5:4-6, Fig. 3B (reproduced below in part, annotated). This “buffer device 350 [(red)] transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360 [(green)].” *Id*. at 6:12-15.



117. Thus, Perego discloses "*a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board*," as recited by Claim 16.

d) *[16.b.i]* the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

118. Perego discloses to a Skilled Artisan "*the plurality of DDR memory devices having a first number of DDR memory devices* [e.g., four x16 memory devices] *arranged in a first number of ranks* [e.g., four ranks]." For example, Perego discloses "grouping memory devices into multiple independent target subsets (i.e. more independent banks)," and a Skilled Artisan would have understood that such groups of "independent target[s]" correspond to a "*first number of ranks*." EX1035 (Perego) at 15:37-45; *supra* ¶¶73-77 (construing "rank").

119. As an example, Perego discloses a "normal memory read operation, [when] buffer device 350 receives control, and address information from controller

310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370. One or more of memory devices 360 may respond by transmitting data to Buffer device 350 which receives the data via one or more of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320a." EX1035 (Perego) at 6:15-24. Perego further explains, that the "address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction." *Id*. at 14:63-65.

120. A Skilled Artisan would have understood from this disclosure that, in the context of DDR SDRAM devices, the "[o]ne or more memory devices," which respond to control and address information by transmitting data through the "target subset of channels 370" during a memory (e.g., read) operation, correspond to one "rank." *See supra* ¶¶73-77 (construing "rank"). Indeed, "rank" refers to an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module. *Id*. A Skilled Artisan would have understood that, for DDR SDRAM devices, such command signals include chip select signals that "provide[] for external Rank selection on systems with multiple Ranks." EX1029 (JESD79-2) at p.6.

121. Perego also discloses implementations where "a maximum buffer device interface width equivalent to the number of data pins or contacts provided on the buffer device's package" (W_{DP}) is the same as the "maximum memory device access width [(W_A)] defined as the largest number of bits that can be accessed in a single memory device transfer operation." EX1035 (Perego) at 14:16-31. A Skilled Artisan would have understood from this disclosure that, for DDR SDRAM devices, the width of the data transaction for a read or write command ("the largest number of bits that can be accessed in a single memory device transfer operation") can be the same as the full width of the memory module ("a maximum buffer device interface width equivalent to the number of data pins or contacts provided on the buffer device's package"), as required for a "*rank*" of memory devices. Thus, a Skilled Artisan would have understood that the number of subsets of memory devices, each subset having "[o]ne or more memory devices" participating in a data transaction in Perego, corresponds to the claimed "*first number of ranks*."

122. To the extent one might argue that Perego does not sufficiently disclose the claimed ranks, it would have been obvious to a Skilled Artisan at least in light of Amidi. As discussed immediately above, Perego discloses that not all the memory devices on the module participate in a data transaction during a read or write command, and the width of the data transaction can be the same as the width

of the memory module. EX1035 (Perego) e.g., at 6:15-24, 14:16-31. Perego also discloses using DDR SDRAM memory devices. *Id*. at 8:1-4, 10:56-59. Amidi discloses that DDR SDRAM memory devices can be organized in multiple ranks on a memory module, where each rank has the same data width as the module and can be selected to participate in a data transaction by a respective chip select signal. EX1036 (Amidi), *e.g.*, at [0003-4], [0034-35] & Fig.3. A Skilled Artisan would have understood that organizing DDR SDRAMs into multiple ranks was a well-known reliable technique at the time for selecting memory devices that participate in a data read or write transaction. For example, a Skilled Artisan would have understood that the chip select signal of DDR SDRAMs was designed for rank selection. EX1029 (JESD79-2) at 6 (explaining that chip select signal "provides for external Rank selection on systems with multiple ranks"); EX1032 (JESD21-C) at 4.20.4-10 through -16 (showing modules with one or two ranks (called "physical banks"), each rank receiving the same chip select signal and having a data width that is same as the width of the memory module). Accordingly, a Skilled Artisan would have been motivated to organize the DDR SDRAM devices in Perego's module into multiple ranks such that each rank receives a respective chip select signal and has the same width as the memory module as taught by Amidi.

123. As discussed above, Perego and Amidi are analogous art to the '912 Patent as each is directed to memory modules that can include memory devices that are different from the memory devices seen by the memory controller. *Supra* ¶¶96-106. Therefore, to the extent one might argue that Perego does not sufficiently disclose the claimed "*ranks*," a Skilled Artisan would have understood and been motivated to organize the DDR SDRAMs of Perego's module into ranks, as disclosed by Amidi, in order to select the "[o]ne or more memory devices" that participate in a data transaction of a memory read or write operation. The combination would have been well within the level of skill at the time, since a Skilled Artisan would have been familiar with the JEDEC standards designed specifically to organize DDR SDRAMs into ranks on a memory module, *supra* ¶¶ 50-52, and the combination provided a module with multiple ranks, as expected.

124. Furthermore, Perego discloses an embodiment in which its module includes four memory devices that are arranged in four ranks, thus each rank has a single memory device. For example, Perego discloses embodiments in which each memory device has its own dedicated channel to receive and transmit data to and from the buffer circuit during a memory operation. EX1035 (Perego) at 10:17-20 ("It is conceivable that if each channel and memory device interface is made narrow enough, then a dedicated channel between each memory device and the buffer device may be implemented on the module."). Perego also discloses that, in

a normal read operation, it is possible for only one memory device to transmit read data through one of the channels. *Id*. at 6:15-24 ("In a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to ***one*** or more, or all of memory devices 360 via channels 370. ***One*** or more of memory devices 360 may respond by transmitting data to Buffer device 350 which receives the data via one or more of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320a.") (emphases added). I have illustrated such an implementation of Perego in a modified version of FIG. 4B (below), where each of channels 415a-d is coupled to a single respective DDR memory device (instead of four memory devices per channel). Here, in each of channels 415a-d, the Buffer 405 interfaces with the respective memory device using the control (RQ), data (DQ), data strobe (DQS), and clock (CK) signals in accordance with the JEDEC DDR standards.

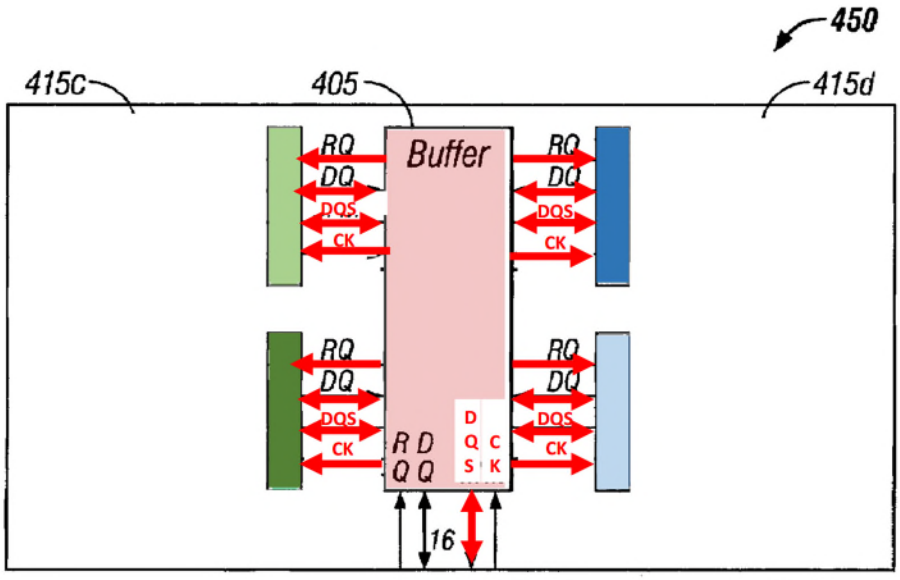


FIG. 4B

Thus, I have also modified Fig. 4B such that the connections to the memory devices correspond to the known signaling of DDR2 memory devices as disclosed by Perego. EX1035 (Perego) at 9:58-60 ("control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines"), 14:4-10 ("In another embodiment of the present invention, an additional complement data strobe signal for each byte of each memory device may be programmed at interfaces 520a and 520b to accommodate different types of memory devices on a configurable width memory module 395, such as legacy memory devices that require such a signal."), 10:56-67 ("Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer device 405 between the memory devices and controller in

accordance with the present invention (e.g., see FIG. 3) may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation."), 10:5-13 (explaining that each channel includes the functionalities of a clock signal, similar to the clock signal CK of DDR devices, as well as source synchronous data transfer, similar to the data strobes DQS of DDR devices); *see also* EX1029 (JESD79-2) at p.6 (Input-Output functions for DDR2 memory devices, including data strobe signals (DQS) and clock signals (CK)).

125. In this implementation of Perego, the "*first number of DDR memory devices*" is four and each memory device has a width of 16 bits (Memory Device Access Width, W_A), just like the width of the memory module (Buffer Device Interface Width, W_{DP}). *See* EX1035 (Perego), *e.g.*, at 14:12-15 (explaining that interfaces 520a and 520b can connect to four "x16" memory devices), 14:16-40 (explaining the relationship between W_{DP} and W_A, including that the interface width W_{DP} and the access width W_A can both be 16 bits); *see also id*. at Fig. 5B (listing 16 as a possible bit width W_{DP} of the module). Accordingly, this implementation of Perego has four ranks ("*first number of ranks*"), each rank having a width of 16 bits. Such a module could be used, for example, in the

system illustrated by FIG. 7 of Perego (reproduced below with modifications to show the implementation where only one 16-bit wide memory is coupled to each channel of the Buffer). EX1035 (Perego) at 20:65-21:3 ("With reference to FIG. 7 and FIG. 4B, a block diagram of a memory system employing a buffered quad-channel module according to an embodiment of the present invention is illustrated. Memory systems 700 incorporate quad-channel modules 450a–450d, each coupled via point-to-point links 620a–620d respectively.").

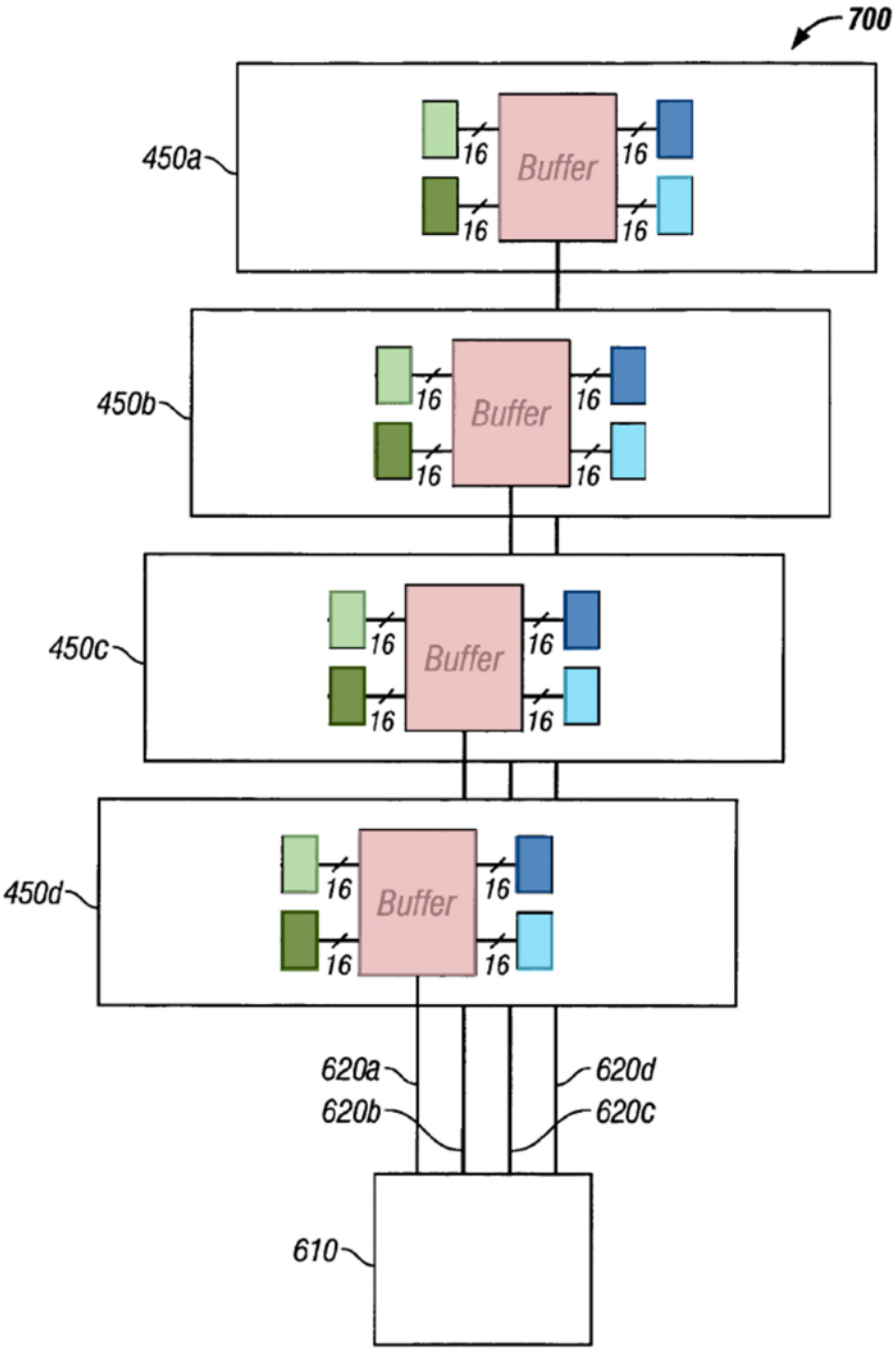


FIG. 7

126. Thus, Perego discloses and renders obvious alone or in view of Amidi to a Skilled Artisan that "*the plurality of DDR memory devices hav[e] a first*

number of DDR memory devices arranged in a first number of ranks;" as recited by Claim 16.

e) *[16.c]* <u>a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,</u>

127. <u>Perego</u> discloses "*a circuit* [e.g., buffer device 405] *coupled to the printed circuit board, the circuit comprising a logic element and a register*."

128. <u>Perego</u>'s buffer device is a "*circuit*" and, as discussed above, it is coupled to the PCB (printed circuit board). *Supra* ¶¶ 111-112, 116; EX1035 (<u>Perego</u>) at 5:56-67. <u>Perego</u> discloses that the buffer device includes a "*logic element*," including request & address logic 540, that translates a protocol employed by the system memory controller into a protocol that is used by the memory device. EX1035 at 10:59-68 ("Utilizing buffer device 405 between the memory devices and controller in accordance with the present invention (e.g., see FIG. 3) may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation."); *see also* FIG. 4B (showing that the signals received by the buffer device include control and address lines, RQ), 9:58-60 ("control lines (RQ) may comprise individual control lines, for example, row address strobe, column

address strobe, etc., and address lines"). In particular, Perego's Fig. 5B discloses that the logic 540 within the buffer device provides the control and address lines (RQ) to the memory interfaces 520a and 520b based on signals received from configurable interface 590. *Id*. at Fig. 5B (reproduced below with annotations). For example, Perego discloses that, in configurable width interface 590, "control information and address information may be decoded and separated from multiplexed data and provided on lines 595 to request & address logic 540 from interface 596." *Id*. at 13:54-59.

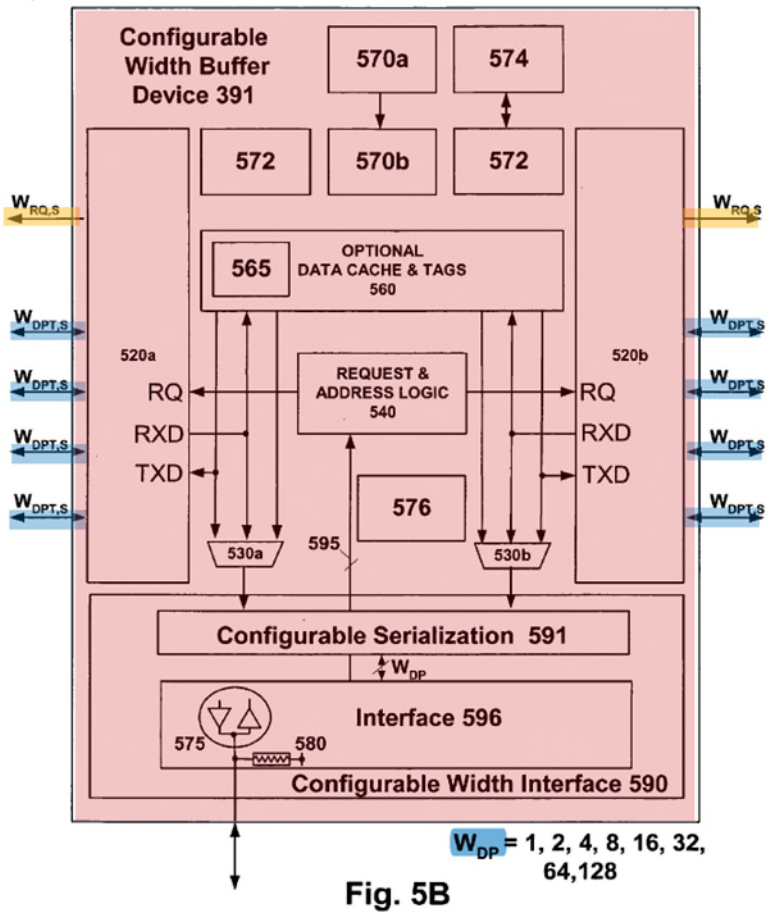


Fig. 5B

129. Perego also discloses to a Skilled Artisan that its buffer device includes a "*register*" which "tranceives and provides isolation" of address, command, and data signals between the memory controller and the memory devices on the module. EX1035 at 6:12-27 ("With further reference to FIGS. 3A and 3B, buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360."). As discussed above, Perego also discloses that interface 596 within the buffer device decodes control and address information. *Id*. at 13:54-59. A Skilled Artisan would have understood from this disclosure that Perego's interface 596 includes registers which latch the received address, command and data signals in order to provide "isolation" and for decoding the control and address information. *See, e.g., id*. at FIG. 5C and 17:61-63 (disclosing latches 597f-m for registering data signals). Furthermore, a Skilled Artisan would have understood that Perego's "buffered module" registers the control and address signals similar to the registered modules of the time. EX1032 (JESD21-C) at 4.20.4-10 through 16 (showing memory modules with registers for registering the received control and address signals).

130. To the extent one might argue that Perego does not sufficiently disclose the claimed "*register*," it would have been obvious to a Skilled Artisan at least in light of Amidi. As discussed above, Perego discloses that its module

includes a buffer that isolates the memory devices from the control and address signals received from the system memory bus. EX1035 (Perego), e.g., at 6:12-27. Amidi, in the same field of memory modules, discloses using a register that performs this functionality. EX1036 (Amidi) at [0038] ("The register 408 is used to synchronize the incoming address and control signals with respect to differential clock signals 208 (clk and clk_n). Also, the register 408 may eliminate the loading of 36 devices in case of stacking or loading of 18 devices in case of monolithic memory devices from the main controller by separating the controller side signaling with memory side signal loading fan-out."). Using such a register in memory modules was also well known at the time. EX1032 (JESD21-C) at 4.20.4-10 through 16 (showing standardized memory modules with registers for registering the received control and address signals). As discussed above, Perego and Amidi are analogous art to the '912 Patent. *Supra* ¶¶96-106. Therefore, a Skilled Artisan would have been motivated to use the functionality of Amidi's register in order to synchronize the incoming address and control signals with the local clock signal, and eliminate the loading effects of the memories from the system bus, thus improving performance. Since this technology was already standardized, the result of the combination was as expected, a registered memory module.

131. Thus, Perego discloses and renders obvious in light of Amidi "*a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,*" as recited by Claim 16.

f) *[16.c.i]* the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,

132. Perego discloses to a Skilled Artisan "*the logic element* [including request & address logic 540 in Perego's buffer device] *receiving a set of input signals* [e.g., signals associated with a read or write command per the JEDEC standard, EX1029,6,49] *from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal* [per the JEDEC standard for DDR memory devices, EX1029,6,49&n.2 (A0-A15[1],BA0-BA2,CS)]." When Perego's computer system is configured to control memory modules with DDR SDRAM devices, the set of input signals comprises at least one row/column address signal, bank address signals, and at least one chip-select signal.

[1] A10 is used for a command signal, rather than an address signal, for certain commands, such as Precharge, Write, and Read. EX1029,6,7-8,33-34,37,49.

133. For example, Perego discloses that "control information and address information may be decoded and separated from multiplexed data and provided on lines 595 to request & address logic 540 from interface 596." EX1035 (Perego) at 13:54-59, FIG. 5B; *see also* FIG. 4B (showing that the signals received by the buffer device include control and address lines, RQ).

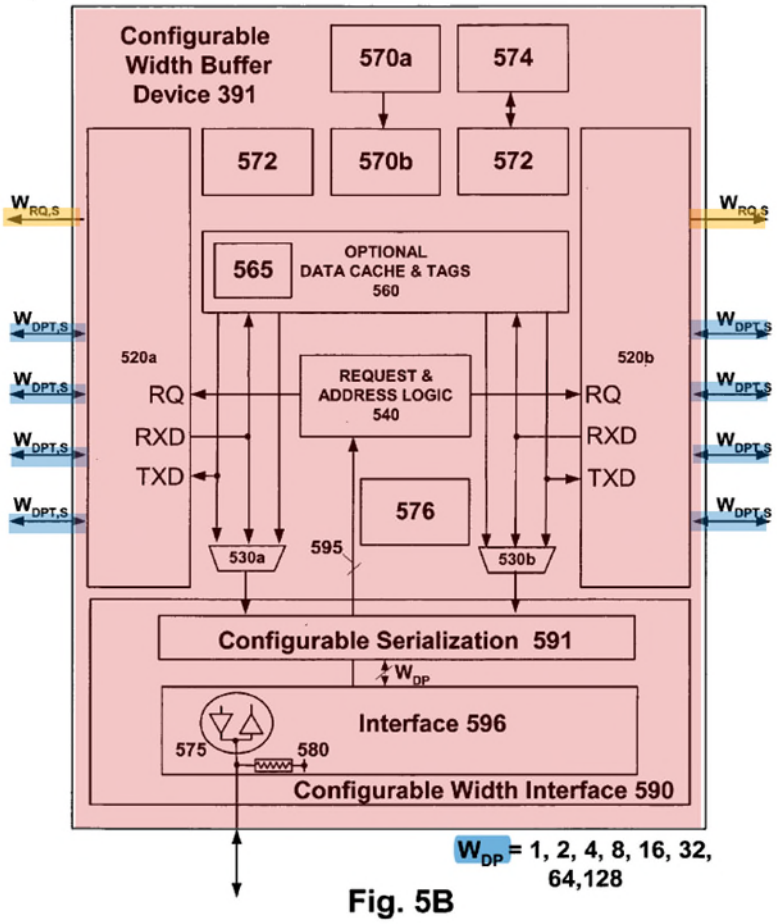


Fig. 5B

134. Perego further discloses that "control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines." EX1035 (Perego) at 9:58-60, *see also id*. at 6:15-19 ("In a

normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370."). A Skilled Artisan would have understood that, for DDR memory devices, the "address lines" (and "address information") in Perego convey both row/column addresses and bank addresses. *See, e.g.*, EX1029 (JESD79-2) at p.6 (listing Bank Address Inputs BA0-BA2 for activate, read, write, and precharge commands and Address Inputs A0-A15 to provide (i) the row address for an activate command and (ii) the column address for read/write commands); p.49 (command truth table, same); EX1036 (Amidi) at [0030-31] & Fig. 2 (disclosing that a standard stacked DDR Device is coupled to an Address Bus, including address lines Address[n:0] and Bank Address lines BA[1:0], and a Control Bus, including RAS, CAS, WE and chip select lines cs[1:0]). Indeed, as discussed above, ¶¶114-117, Perego discloses that "memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices." EX1035 (Perego) at 10:56-59; *see also id*., 3:67-4:3 ("Examples of types of memory devices include dynamic random access memory (DRAM), static random access memory (SRAM), and double data rate SDRAM (DDR)."), 8:1-9 ("In the described embodiment, memory devices 360 are discretely packaged Synchronous type DRAM integrated circuits (ICs), for

example, DDR memory devices, …"). Thus, a Skilled Artisan would have understood that "control information and address information" provided to the request and address logic 540 ("*the logic element*") include "*at least one row/column address signal, bank address signals, and at least one chip-select signal*" in the case of DDR SDRAM devices, because these signals are part of the standard input/output functions of DDR SDRAM devices. *See, e.g.*, EX1029 (JEDEC standard for DDR2 memory devices) at p. 6 (reproduced below); *see also id.* at p.49 (showing the use of those signals, e.g., for Bank Activate, Read, and Write commands); EX1032 (JEDEC 21-C) at 4.20.4-6 (pin description of registered memory modules, disclosing same).

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$) (UDQS), ($\overline{UDQS}$) (LDQS), ($\overline{LDQS}$) (RDQS), ($\overline{RDQS}$)	Input/Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and $\overline{RDQS}$ may be used in single ended mode or paired with optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$, and RDQS to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.

135. Furthermore, as discussed below in more detail with reference to claim elements **[16.c.ii], ¶¶137-165, and [16.c.iii], ¶¶166-168**, a Skilled Artisan would have understood that the logic element needs "*at least one row/column address signal, bank address signals, and at least one chip-select signal*" in order "to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation," so that the module can use different DDR SDRAM devices than what is expected by the memory controller. EX1035 (Perego) at 10:63-68.

136. Thus, Perego discloses "*the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,*" as recited by Claim 16.

g) *[16.c.ii]* the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,

137. Perego discloses to a Skilled Artisan "*the set of input signals configured to control a second number of DDR memory devices* [e.g., two x8 memory devices] *arranged in a second number of ranks* [e.g., one rank], *the second number of DDR memory devices* [e.g., two x8 memory devices] *smaller than the first number of DDR memory devices* [e.g., four x16 memory devices] *and the second number of ranks* [e.g., one rank] *less than the first number of ranks* [e.g., four ranks]."

138. For example, Perego discloses that "[d]ifferent types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation." EX1035 (Perego) at 10:63-67. Perego further discloses that memory systems can use "x4"

(i.e., 4-bit wide), "x8" (8-bit-wide), and "x16" (16-bit-wide) memory devices. *Id.* at 14:12-15 ("For example, interfaces 520a and 520b may be programmed to connect to 16"x4" width memory devices, 8"x8" width memory devices or 4"x16" width memory devices."). Memory devices with these bit-widths had been standardized by JEDEC. EX1030,4-6;EX1034,1-2,20;EX1029,7. Perego also teaches that "the buffer device may be a configurable width buffer device to provide upgrade flexibility." *Id*. at 3:25-28.

139. A Skilled Artisan would have understood from this disclosure that, by using Perego's protocol translation, its module can include x16 memory devices to upgrade a memory system that is configured for memory modules with x8 memory devices. Indeed, it was common at the time that memory modules could include x8 memory devices, *see, e.g.*, EX1032 (JEDEC 21-C) at 4.20.4-13, -25 to -26 (examples of modules with x8 memory devices), and some memory systems with multiple modules had control only for one or two ranks per module, *see, e.g.*, EX1036 (Amidi) at [0004] ("Standard memory modules such as memory module 106 have either one rank or two rank of memory devices"). Therefore, a Skilled Artisan would have understood that Perego's translation protocol allowed use of a memory module with x16 memory devices in a system configured to control memory modules with one rank of memory devices (e.g., two x8 memory devices in the rank). EX1035 (Perego) at 10:14-17 (disclosing that the number of

channels, and thus the corresponding number of ranks, can be one, two, or more). As discussed above, Perego also discloses that such a module can be 16 bits wide. EX1035 at Figs. 4B and 7 ("/16" indicating a data width of 16 bits) and Fig. 5B (expressly listing 16 as the bit width W_{DP} of the module).

140. Furthermore, a Skilled Artisan would have also understood that there was a trend at the time of Perego and the '912 Patent to increase the data width of the memory devices. This is evident in writings of the day. *See, e.g.*, EX1034 at 20 ("To achieve higher bandwidth per DRAM, the trend in recent years has been not only to increase DRAM speed but also increase the number of data-out pins: x32 parts are now common. Every increase from x4 to x8 to x16 and so on doubles the DRAM's data rate. Doubling the data rate by doubling the data width of existing parts requires very little engineering know-how. It only requires the addition of more pins and doubling the width of the data bus to each individual DRAM."). A Skilled Artisan would have also understood that using the latest generation of high-capacity memory devices to build a high-capacity memory module was expensive at the time. EX1036 (Amidi) at [0008] ("Because memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices.").

141. Therefore, a Skilled Artisan would have been motivated to make a high-capacity memory module using the same generation of lower-capacity

memory devices instead of using the next generation of higher-capacity memory devices, and those lower-capacity memory devices can include x16 memory devices. For example, a Skilled Artisan would have been motivated to use four ranks of low density x16 memory devices instead of one rank of high-capacity x8 memory devices. *See, e.g.*, EX1035 (Perego) at 3:23-25 ("In several embodiments, the buffer device provides for flexible system configurations, and several performance benefits."). Furthermore, in light of the finite number of different memory device bit-widths at the time, it would have been obvious to try this specific combination. *See, e.g.*, EX1036 (Amidi) at [0004-0005] ("For example, a single 128 Mbit DDR SDRAM family comes in three flavors of [bit width x4, x8, and x16] … One can build memory modules with similar densities using different data bits flavors.").

142. A Skilled Artisan would have understood at the time that Perego's disclosure was written such that a 16-bit wide one-rank memory module with a total capacity of 1Gb can be formed with two 64Mb x8 ("by eight," i.e., eight-bit wide) DDR2 memory devices each 512Mb (blue box) in that rank. EX1029 (JESD79-2) at p.7 (Tables 2 and 3 reproduced below with annotations); *see also* EX1032,4.20.4-11,-29 (showing how x8 memory devices can be combined in a rank to create a larger bit-width for the module).

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

In such a one-rank 1Gb module, accessing a specific memory location requires 14 row address bits (A_0-A_{13}), 10 column address bits (A_0-A_9), and two bank address bits (BA0, BA1). *Id*. (as shown by the configuration parameters in the blue box). To double the capacity of such a one-rank module to 2Gb, the two 64Mbx8 (eight-bit wide) DDR2 memory devices (blue box) can be replaced by two 128Mbx8 (eight-bit wide) DDR2 memory devices (red box), requiring three bank address bits (BA0-BA2) instead of two, while using the same number of row and column address bits. *Id*. A Skilled Artisan, however, would have also understood at the time that, to implement the one-rank module with double (2Gb) capacity, using two x8 memory devices with 1Gb capacity each may not be the best option, because those memory devices may not be available or they may be too expensive. EX1036 (Amidi) at [0008] ("Because memory devices with lower densities are

cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices.").

143. Thus, a Skilled Artisan would have been motivated to look for other options. A Skilled Artisan would have been familiar with the standards of the day, *supra* ¶¶ 50-52, and would have understood that, following the trend at the time of Perego's disclosure, the capacity of the one-rank module can be also doubled to 2Gb by using wider, lower (e.g., 512Mb) capacity memory devices, such as four 16-bit wide 32Mb x16 memory devices (green box above). EX1029 (JESD79-2) at 7 (Tables 2 and 3 reproduced above with annotations). Indeed, Amidi expressly teaches that memory modules can be built using different "flavors" of memory devices, including different bit widths. EX1036 (Amidi) at [0004-5] ("For example, a single 128 Mbit DDR SDRAM family comes in three flavors of [x4, x8, and x16] … One can build memory modules with similar densities using different data bits flavors."), [0008] (teaching that "lower densit[y] devices" are "cheaper and more readily available").

144. A Skilled Artisan would have also understood that, to behave like one 16-bit wide rank, Perego's module can advantageously use four x16 memory devices (32Mb x16, green box) instead of, say, four x8 memory devices (64Mb x8, blue box), because using x16 memory devices would have been beneficial in terms of power consumption and performance. EX1035 at 15:40-45 ("By accessing a

subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks).”). Indeed, a Skilled Artisan would have understood that, by using four ranks of x16 memory devices instead of two ranks x8 memory devices (with two memories in each rank), power consumption is decreased because the number of memory devices (chips) activated in a single cycle is decreased. For example, only one x16 memory device participates in a single read or write operation, instead of two x8 memory devices. Similarly, a Skilled Artisan would have understood that, by using four ranks of x16 memory devices instead of two ranks x8 memory devices, performance is increased because of the increase in the number of pages that can be open at one time and, in some cases, increased page size. In the example discussed above, each x8 memory device of 512Mb capacity (blue box) has a page size of 1kB (where ‘B’ refers to one byte, i.e., 8 bits). EX1029 (JESD79-2) at p.7 (reproduced above in part, annotated). In contrast, each x16 memory device of 512Mb capacity (green box) has a page size of 2kB, therefore doubling the page size that is available for quick access. *Id*.

145. Furthermore, a Skilled Artisan would have also been motivated to use four 32Mb x16 memory devices (green box) instead of two 128Mb x8 memory

devices (red box), because each 32Mb x16 memory device has a smaller capacity (512Mb) than one 128Mbx8 device (1Gb). EX1029 (JESD79-2) at p.7 (reproduced above in part, annotated). Thus, using such x16 memory devices may have also been cheaper at the time. EX1036 (Amidi) at [0008] ("Because memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices."). Indeed, these same market forces appear to have been what motivated the (later) named inventors of the '912 Patent. EX1001 at 4:59-5:5 ("Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.").

146. I further note that the above example of Perego's module using four x16 memory devices to behave like one rank of two x8 memory devices is just that, an example. As I discuss in detail below with reference Ellsberry, other examples were also obvious to a Skilled Artisan at the time, including the '912 Patent's Example 2 where two memory devices of a given bit width emulate a higher-capacity memory device of the same bit width. EX1001 at cols.18-19. Indeed, Amidi expressly discloses such an example. EX1036 at [0046-48].

147. Thus, to the extent the '912 Patent's Example 2 supports claim 16, *infra* at ¶¶ 173-174, such a row-address based rank multiplication would have also been obvious. Indeed, a Skilled Artisan would have been motivated to implement Amidi's rank multiplication functionality in Perego's module in a similar manner, by including four memory devices ("*first number of memory devices*") arranged in four ranks ("*first number of ranks*") and communicating with the system controller like a module with two memory devices ("*second number of memory devices*") arranged in two ranks ("*second number of ranks*"). *Supra* at ¶¶96-106, *see, e.g.*, Ex1036 (Amidi) at [0008] ("Because memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices."). In the example where each rank has one x16 memory device, this implementation of Perego and Amidi can use the two x16 memory devices on the left (light and dark green) to

selectively respond to input signals directed to one (virtual) higher-capacity memory device, and the two x16 memory devices on the right (light and dark blue) to selectively respond to input signals directed to another (virtual) higher-capacity memory device.

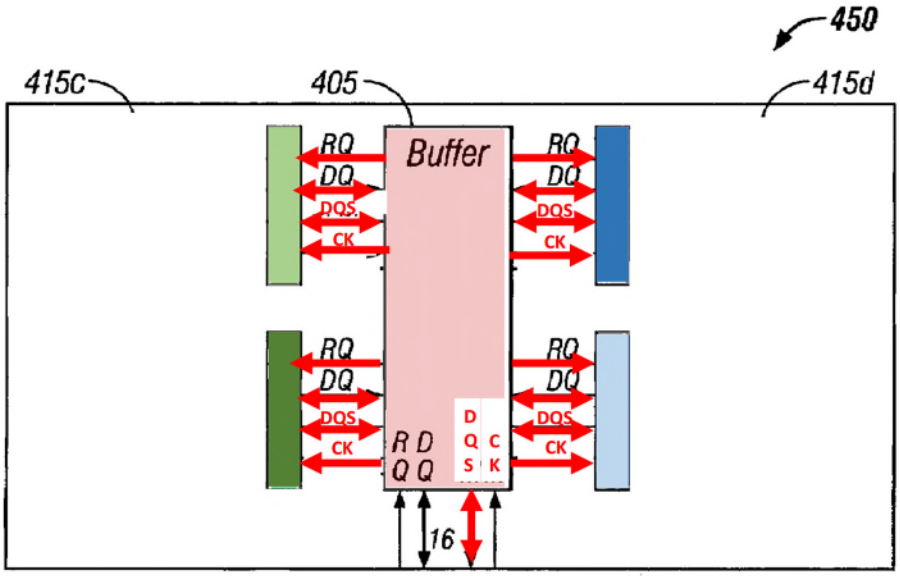


FIG. 4B

148. For example, a Skilled Artisan would have been motivated to build Perego's 16-bit wide module with four x16 memory devices for a system where the memory controller can control only two ranks per module as taught by Amidi, and she would have understood that Perego's module can use the extra row address bit A13 (orange) received for a (virtual) 128Mb x16 memory device (red box) to select between two 64Mb x16 memory devices (blue box) as the target of a memory read or write operation. *Compare* EX1036 at [0049] ("However, the size of the row address for the 128 Mbit DDR SDRAM differs by one row address line

from the 256 Mbit DDR SDRAM (A12). The CPLD 410 uses a Row Address Decoding scheme to emulate a two rank based on 256 Mbit DDR SDRAM Device Technology memory module with a four rank based on 128 Mbit DDR SDRAM Device Technology memory module."); EX1029 at p.7 (reproduced below, annotated).

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 4 — 2Gb Addressing

Configuration	512Mb x4	256Mb x 8	128Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A14	A0 ~ A14	A0 ~ A13
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

149. For the sake of clarity, below I focus on the first example, where a four-rank 2Gb module with one x16 memory device in each rank looks to the system memory controller like a one-rank 2Gb module with two x8 memory devices, but the principles I discuss apply equally to other examples, including the second example above of two x16 memory devices responding to signals directed to a higher-capacity x16 memory device.

150. Implementing such a four-rank 2Gb module with one x16 memory device in each rank that looks to the system memory controller like a one-rank 2Gb module with two x8 memory devices was well within the level of skill at the time. Indeed, as shown by the JEDEC standard below, 32Mbx16 memory devices (green box) are accessed by the same column address bits (A_0-A_9) as the 128Mbx8 memories (red box), but require one less (13) row address bits (A_0-A_{12}) and only two bank address bits (BA0, BA1). EX1029 (JESD79-2) at p.7 (reproduced below in part, annotated).

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Thus, even in a system where the memory controller can address only one rank of two x8 memory devices, a Skilled Artisan would have understood that the extra address bits — in this example row address bit A_{13} and bank address bit BA2 — can be used to "determine which target subset of channels 370 will be utilized for

the data transfer portion of the transaction." EX1035 (Perego) at 14:62-65. For example, a Skilled Artisan would have understood that, in order to perform a read or write operation, first a Bank Activate command is received with the row and bank address signals. EX1029 (JESD79-2) at p.49 & n.2 (reproduced below in part). A subsequent read or write command is received with corresponding bank address signals (but without the row address). *Id*.

Table 10 — Command truth table.

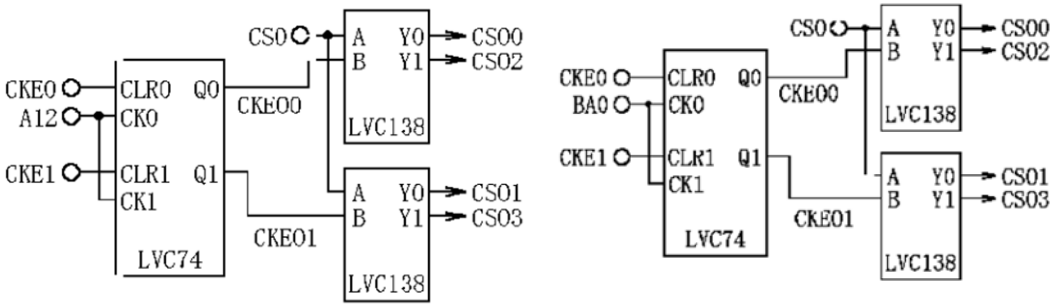
Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Thus, a Skilled Artisan would have understood that the target memory device and its target memory bank is selected in accordance with the bank address signals of the read or write command and the previously received row address and bank address signals of the activate command. *Id*. at NOTE 2 ("Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon").

151. Indeed, a Skilled Artisan would have understood how to identify and use the differences in the address spaces of the physical and emulated devices to

generate additional chip select signals for the additional ranks of the module. *See, e.g.*, EX1036 (Amidi) at [0047-49, 55-57] (comparing the address spaces of the physical memories of the module and the emulated memories as seen by the memory controller to determine the address bit used to generate additional chip select signals for selecting the target subset of the physical memory ranks), and EX1042 (Masashi) at [0010] (explaining that the address bit A12 is used to address a 32 Mbit×8 bit DRAM1 device, but A12 is not used to address a 16 Mbit×4 bit SDRAM2, so this extra address bit A12 can be used to generate chip select signals for controlling multiple 16 Mbit×4 bit SDRAMs emulating a 32 Mbit×8 bit DRAM1 device) & Fig. 1 (reproduced in part below, left, showing the generation of additional chip select signals based on A12); *see also id*. at [0020] (explaining that an input bank address signal BA0, directed to a virtual higher-capacity memory device, can also be used to generate the additional chip select signals for physical memory devices which have only a single bank and thus no bank address signal inputs) & Fig. 4 (reproduced below, right, showing the generation of additional chip select signals based on BA0).



152. To the extent one might argue that Perego alone does not sufficiently disclose or render obvious this limitation, it would have been obvious to a Skilled Artisan in light of Amidi. *Supra* ¶¶96-106. This combination of Perego with Amidi would have been obvious to a Skilled Artisan for reasons explained generally above and specifically in relation to this limitation below. *Id*.

153. For example, Amidi discloses "a transparent four rank memory module fitting into a memory socket having two chip select signals routed" including "[a]n emulator coupled to the memory module [which] activates and controls one individual memory rank from either the first memory rank, the second memory rank, the third memory rank, or the fourth memory rank based on the signals received from a memory controller." EX1036 (Amidi) at [0011-12] & FIG. 6A. Therefore, it would have been obvious to a Skilled Artisan to implement the protocol translation in Perego's module to include the functionality of an emulator that "activates and controls one individual memory rank" out of four memory ranks based on control signals for less than four ranks as taught by Amidi, because that would reduce the cost of a high-capacity module compared to a module of the same high-capacity implemented with higher-capacity memory devices.

154. A Skilled Artisan would have also been motivated to look at Amidi's transparent memory module and its improvements because both Amidi and Perego disclose a transparent memory module. EX1035 (Perego) at 10:59-67 ("Utilizing

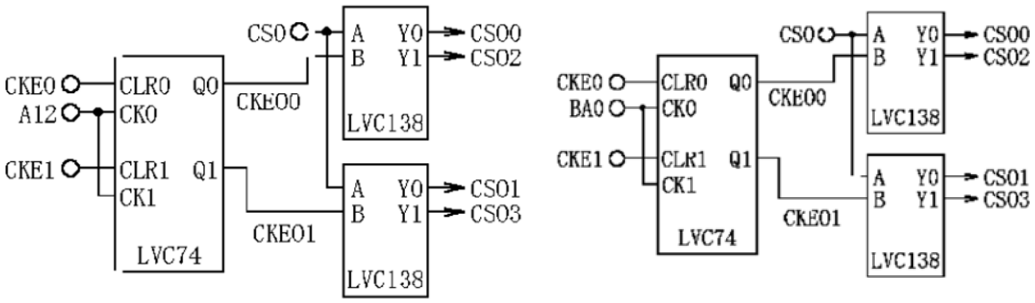
buffer device 405 between the memory devices and controller in accordance with the present invention (e.g., see FIG. 3) may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation."); *see also* EX1036 (Amidi) at Abstract ("A transparent four rank memory module has a front side and a back side. The front side has a third memory rank stacked on a first memory rank. The back side has a fourth memory rank stacked on a second memory rank. An emulator coupled to the memory module activates and controls one individual memory rank from either the first memory rank, the second memory rank, the third memory rank, or the fourth memory rank based on the signals received from a memory controller."). Therefore, a Skilled Artisan would have been motivated to look at Amidi's rank multiplication technique to implement the protocol translation of Perego for DDR SDRAM devices.

155. Furthermore, both Perego and Amidi teach using the address signals to select the target rank. *See, e.g.*, EX1036 (Amidi) at [0043-44] & FIG. 5; EX1035 (Perego) at 15:31-45 ("According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request. By accessing a subset of secondary channel

signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks).”). In addition, a Skilled Artisan would have been motivated to double the width of the memory devices on the module (in relation to the memory devices the system memory controller recognizes), because “[d]oubling the data rate by doubling the data width of existing parts requires very little engineering know-how.” EX1034 at 20. As further discussed above, using four ranks of x16 memory devices instead of two ranks of two x8 memory devices in each rank would save power and increase performance. *Supra* at ¶144.

156. To the extent one might argue that Amidi does not disclose that the “*logic element*” receives the claimed “*bank address signals*” as part of the “*set of input signals*,” Perego, alone or in combination with Amidi, teaches this when Perego discloses that request & address logic 540 (which is part of the claimed “*logic element*”) receives control and address information, which a Skilled Artisan would have understood include bank address signals for DDR SDRAM devices. *See, e.g.*, EX1035 (Perego) at 13:54-59 (“For example, control information and address information may be decoded and separated from multiplexed data and provided on lines 595 to request & address logic 540 from interface 596.”); *see also* EX1029 (JEDEC standard for DDR2 memory devices) at pp. 6, 49&n.2.

157. As also discussed above, a Skilled Artisan would have understood that Perego's request & address logic 540 can use both a row address signal (received with a Bank Activate command) and bank address signals (of the Bank Activate and Read or Write commands) to select the target x16 memory device for the data transaction. Indeed, a Skilled Artisan would have understood that both row address and bank address signals can be used to generate additional chip select signals. *See, e.g.*, EX1042 (Masashi) at [0010] (explaining that the address bit A12 is used to address a 32 Mbit×8 bit DRAM1 device, but A12 is not used to address a 16 Mbit×4 bit SDRAM2, so this extra address bit A12 can be used to generate chip select signals for controlling multiple 16 Mbit×4 bit SDRAMs emulating a 32 Mbit×8 bit DRAM1 device) & Fig. 1 (reproduced in part below, left, showing the generation of additional chip select signals based on A12); *see also id*. at [0020] (explaining that a bank address signal BA0 of a virtual memory device can also be used to generate the additional chip select signals for selecting physical memory devices which have only a single bank and thus no bank address signal inputs) & Fig. 4 (reproduced below, right, showing the generation of additional chip select signals based on BA0).



158. For example, Amidi teaches to a Skilled Artisan that the row address is received before the read or write command, which includes a bank address and column address. Amidi explains that, consistent with the JEDEC standard, "[f]irst, the Row address needs to be provided with the proper control and command signals then on a separate cycle, the Column address needs to be provided with its proper control and command signals in order to read or write to that particular cell." EX1036 (Amidi) at [0061], Fig. 6A; EX1030,1,5,13("Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ***ACTIVE*** command are used to select the ***bank and row*** to be accessed. The address bits registered coincident with the ***READ or WRITE*** command are used to select the ***bank and the starting column*** location for the burst access."); EX1029,49&n.2; *see also* EX1034 at 4 (explaining that first a row of a DRAM array is activated by driving that row into the sense amps, and the subsequent read or write command acts on that row) & Fig. 5 (reproduced below, showing the same).

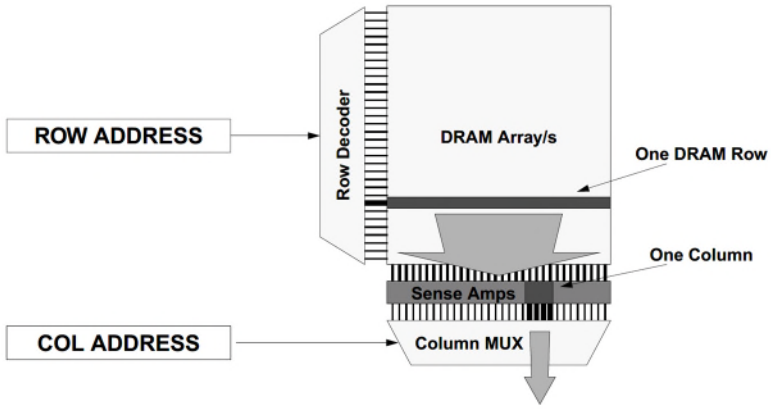


Figure 5: The Multi-Phase DRAM-Access Protocol
The row access drives a DRAM row into the sense amps. The column address drives a subset of the DRAM row onto the bus (e.g., 4 bits).

159. I further note that a Skilled Artisan would have understood that Amidi's teaching that its CPLD uses a row address bit to select the target of a memory read or write operation, EX1036 (Amidi) at [0061], means that Amidi stores that row address bit, because row addresses are received with an earlier Bank Activate command (and the later Read or Write command does not include the row address). EX1030,1,5,13; EX1029 (JESD79-2) at p.49 & n.2 (reprinted below, in part, with annotations); EX1044 (Dell) (US6,209,074) at 8:36-40 ("The ASIC 24 needs to store the BA1 address applicable to each of the BA0 options. This allows the ASIC 24 to re-send the BA1 signal at CAS time to ensure that the correct bank is addressed.").

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Amidi also expressly discloses that its CPLD uses that stored row address bit (along with the chip-select signals) as an input to select the target rank of a read or write operation. EX1036 (Amidi) at Figs. 3, 5, 8 (add(n) input to blocks 812 and 814). Because a Bank Activate command delivering the row address is specific to a bank identified by bank address signals, a Skilled Artisan would have understood — and it at least would have been obvious to her — that Amidi's CPLD 604 uses the bank address signals during Row Address Decoding to store and retrieve row address bits selectively for respective banks.

160. I note that during reexamination (discussed above at ¶¶63-65) the Board found that, based on Amidi's disclosure, it would have been obvious to a Skilled Artisan to store a row address for a subsequent read or write operation that operates on the columns of that row. EX1011 at 56-58 (pp.53-55 of Decision mailed 5/31/2016). In addition, the Board stated that "Dell 2 also teaches that one skilled in the art would have recognized storing signals for later use, including

during a column access procedures, to ensure the correct bank is addressed." EX1011 at 62 (p.59 of Decision mailed 5/31/2016, citing EX1044 (US6,209,074) at 8:36-40).

161. Amidi also explains that, in Row addressing mode, one of the row address bits (Add(n)) is used to select the target rank. EX1036 (Amidi) at [0043], [0047-49], [0052] ("For example, CPLD 604 generates rcs2 and rcs3, besides rcs0 and rcs1 off of CS0, CS1 and Add(n) from the memory controller side."), Fig. 8 (showing OR circuits 812 and 814 receiving "add(n)"). Therefore, a Skilled Artisan would have understood that the row address bit Add(n) is stored when it is first received and the stored value is used later when the read or write command is received.

162. A Skilled Artisan would have also known that bank address signals (BA) determine which internal bank of the target memory device(s) would perform the read or write operation. *Id*. at Fig. 6A; EX1029 at p.49 (Table 10 showing that read and write commands are bank specific, reproduced above in part), *id*. at NOTE 2 ("Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon."). Accordingly, a Skilled Artisan would have understood that, in Amidi's Row Address decoding, the stored row address bit (i.e., add(n)) is specific to a corresponding bank, and that bank is identified by the bank address (BA) signals. Thus, a Skilled Artisan would have understood — and she at least would

have been motivated — to use the bank address (BA) signals to store and retrieve the row address bit (add(n)) for a specific bank, in order to keep track of which row address bit corresponds to which bank when the read or write command arrives.

163. Therefore, a Skilled Artisan would have understood from Amidi's disclosure that a row address bit Add(n) is stored for a corresponding bank when that row address is received with a Bank Activate command, and the stored bank-specific row address bit is used to select the target rank for the later read or write operation for that specific bank. In other words, a Skilled Artisan would have understood, and would have found it obvious, that in Amidi, the bank address signals are received by the logic performing row-address-based rank multiplication in order to store and retrieve the right row address bit for the right bank.

164. Furthermore, as I noted above, *supra* at ¶¶146-148, a Skilled Artisan would have understood that other combinations of memory devices were also possible. For example, the number of channels of Perego's buffer device, thus the number of ranks on the module, is not limited to four, and the number of ranks seen by the memory controller is not limited to one. EX1035 (Perego) at 10: 26-30 ("By incorporating more channels and additional memory devices, module 450 (FIG. 4B) may be implemented in memory systems that require large memory capacity"), 11:52-55 ("In alternate embodiments of the present invention, interfaces 520a and 520b include any number of channels e.g., two, four, eight or

more channels."). For example, in a memory module where the interfaces 520a and 520b have a total of eight channels, with each channel coupled to a x16 DDR SDRAM, and using the same rank multiplication based on row and bank address signals as discussed above, the "*first number of DDR memory devices*" would be eight x16 memory devices, and the "*first number of ranks*" would be eight ranks, emulating a module with two ranks ("*second number of ranks*"), each having two x8 memory devices, providing a total of four x8 emulated memory devices ("*second number of memory devices*").

165. Accordingly, Perego alone or in view of Amidi renders obvious that "*the set of input signals [is] configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,*" as recited by Claim 16.

h) *[16.c.iii]* the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,

166. Perego discloses "*the circuit* [e.g., buffer device 405] *generating a set of output signals in response to the set of input signals, the set of output signals*

configured to control the first number of DDR memory devices arranged in the first number of ranks."

167. Perego discloses, for example, "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370." EX1035 (Perego) at 6:15-19. Perego further discloses that "[d]ifferent types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation." *Id.* at 10:63-67. A Skilled Artisan would have understood from this disclosure that, when Perego's buffer circuit "translate[s] protocols" for the exemplary implementation of four ranks with one x16 memory device in each, it is generating output signals in accordance with the protocol of those of those x16 memory devices, in response to receiving a read command for x8 memory devices, for the reasons discussed above with reference to claim elements **[16.b.i], ¶¶118-126, and [16.c.ii], ¶¶137-165**. *See also* EX1035 (Perego) at Fig. 4B (reproduced below with modifications showing the specific implementation discussed above).

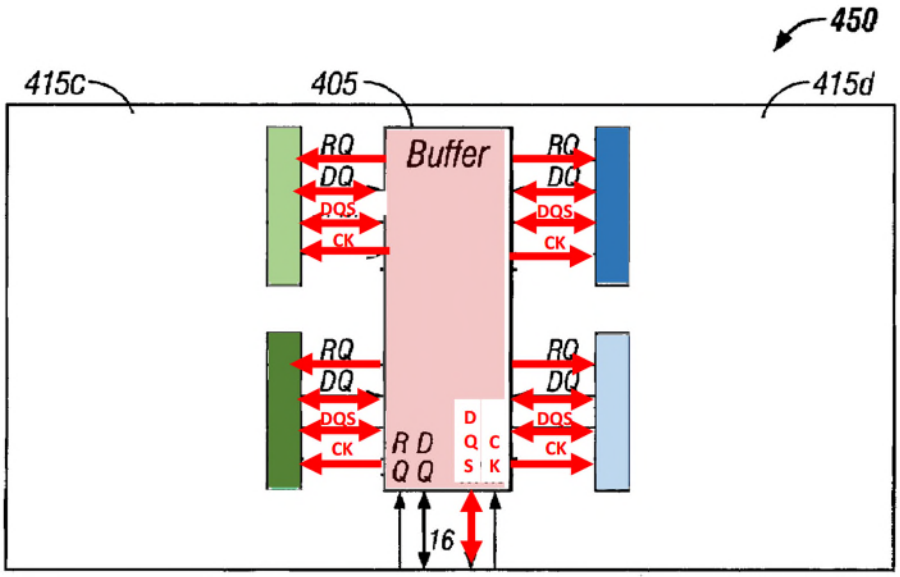


FIG. 4B

168. Thus, Perego discloses and renders obvious in view of Amidi to a Skilled Artisan "*the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,*" as recited by Claim 16.

i) *[16.c.iv]* wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

169. Perego discloses "*wherein the circuit* [e.g., buffer device 405] *further responds to a command signal* [e.g., for a read or write command per the JEDEC standard, EX1029,6,49] *and the set of input signals from the computer system by*

selecting one or two ranks [e.g., one rank] *of the first number of ranks* [e.g., four ranks] *and transmitting the command signal to at least one DDR memory device of the selected one or two ranks* [e.g., one rank] *of the first number of ranks* [e.g., four ranks]."

170. For example, Perego discloses that, "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370." EX1035 at 6:15-19. Therefore, Perego expressly discloses selecting "one" memory device and transmitting the corresponding signals to the selected memory device. As discussed above, a Skilled Artisan would have understood that such a x16 memory device can form one rank, since it can provide the same data width as the width of the memory module. *See also* EX1035 at Fig. 4B (reproduced below with modifications showing the specific implementation discussed above).

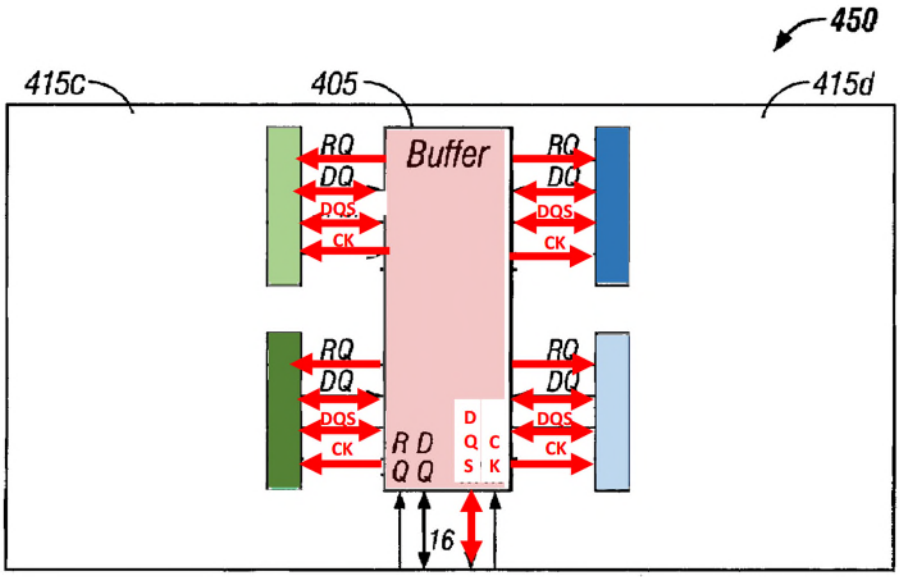


FIG. 4B

171. Perego further explains:

> If the total number of secondary channel signal lines per configurable width buffer device 391, $W_{DP,S}$ is greater than the minimum number required per transaction, $W_{DPT,S}$, then configurable width buffer device 391 may employ a configurable datapath router within interface 591 to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction. According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request. By accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks).

EX1035 (Perego) at 15:31-45. A Skilled Artisan would have understood from this disclosure that the address information received from the memory controller can be used to select the target rank for the memory transaction. A Skilled Artisan would

have also understood that such an implementation has a number of benefits, including more independent ranks, thus increased capacity of the memory module.

172. Furthermore, as discussed above, a Skilled Artisan would have been motivated to use the rank multiplication functionality of Amidi in the memory module of Perego. *Supra* ¶¶96-106. For example, Amidi expressly teaches using a row address signal and chip select signals to select one of the ranks for performing a read or write operation. EX1036 (Amidi) at [0043-44] & Fig. 5. As further discussed above with reference to claim element **[16.c.ii], ¶¶137-165** (especially ¶142), the specific combination of using x16 memory devices on the module (even though the system sends address and control information for one rank having two x8 memory devices) requires selecting one of the ranks in accordance with a row address (including A_{13}) and bank address bits (including BA2) of the Bank Activate and Read or Write commands received from the memory system controller (which include chip-select signals). *See supra* ¶¶137-165 (especially ¶142). Therefore, Perego alone and in view of Amidi discloses to a Skilled Artisan that the selection of the target rank is in response to a command signal, such as a read or write command, and in response to "*the set of input signals*" that includes "*at least one row/column address signal, bank address signals, and at least one chip-select signal*."

173. I note that the '912 Patent itself does not expressly describe selecting the target rank based on both a row/column address and a bank address, meaning that Perego alone and in view of Amidi actually provides a better disclosure of the claimed invention than the '912 Patent itself. In its EXAMPLE 1 code, the '912 Patent discloses "memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit," that is based on a bank address, without any row/column address. EX1001 at 14:17-23. In its EXAMPLE 2 code, the '912 Patent discloses "[a]nother exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit," i.e., without basing the selection on a bank address. *Id*. at 17:28-31. Instead, this example uses the bank address to selectively store that row A_{13} density transition bit. *Id*. at cols. 18-19 (showing that bank address signals bnk0 and bnk1 are used to select one of four registers a13_00, a13_01, a13_10, and a13_11 to store and retrieve the row address bit a_13r). As I explained above, a Skilled Artisan would have understood, for example from the disclosure of Amidi and her knowledge of the relevant JEDEC standards, that a row address density bit is stored selectively for each internal bank of a DDR SDRAM device. *Supra* at ¶¶158-163; *see, e.g.*, EX1029 (JESD79-2) at p.49 n.2 ("Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.").

174. Therefore, to the extent using the bank address signals only for storing the respective row address bit satisfies the claimed selection (similar to EXAMPLE 2 in the '912 Patent discussed above), the combination of Perego and Amidi renders the claim obvious even if the rank selection is based on a row address, since such a row-address based selection also uses the bank address signals for storing that row address. *Supra* at ¶¶146-148, 158-163. For example, a Skilled Artisan would have understood that the row address bit A_{13} is the difference in addressing 64Mbx16 (blue box) and 128Mbx16 (red box) memory devices. *Id.*, *see also* EX1029 (JESD79-2) at 7 (Tables 3 and 4 reproduced below, annotated).

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 4 — 2Gb Addressing

Configuration	512Mb x4	256Mb x 8	128Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A14	A0 ~ A14	A0 ~ A13
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Amidi teaches that, using this row address bit, two smaller capacity 64Mbx16 devices can emulate one 128Mbx16 device. EX1036 [0047-49]. Accordingly, for

the reasons discussed above, a Skilled Artisan would have been motivated to implement the module of Perego with the Amidi rank multiplication functionality, so that four ranks, each having one 64Mbx16 device, emulate two ranks with one 128Mbx16 device in each rank as seen by the system memory controller. *Supra* ¶¶96-106. Thus, in the combination where the module has four ranks as illustrated in the modified Fig. 4B of Perego (below), the system memory controller would see only two ranks.

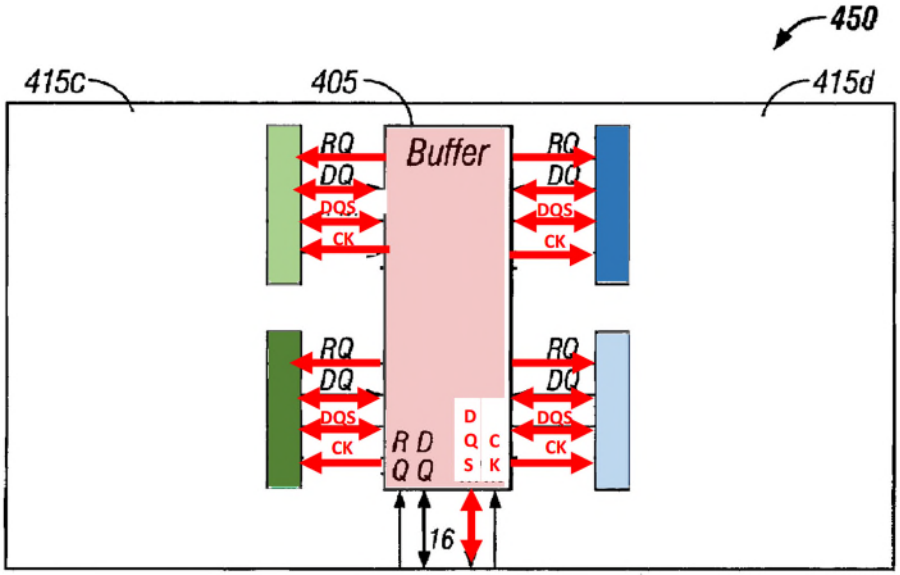


FIG. 4B

175. Thus, Perego discloses and renders obvious in view of Amidi to a Skilled Artisan that "*the circuit further responds to command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory*

device of the selected one or two ranks of the first number of ranks" as recited by Claim 16.

j) *[16.d]* a phase-lock loop device coupled to the printed circuit board,

176. Perego discloses that its module also includes "*a phase-lock loop device coupled to the printed circuit board*."

177. For example, Perego discloses that buffer device 405 includes a "clock circuit 570a–b [which] includes one or more clock alignment circuits for phase or delay adjusting internal clock signals with respect to an external clock (not shown). Clock alignment circuit may utilize an external clock from an existing clock generator, or an internal clock generator to provide an internal clock, to generate internal synchronizing clock signals having a predetermined temporal relationship." EX1035 (Perego) at 12:65-13:5. Perego also discloses that the function of "a phase lock loop (PLL) generator device [is] to generate phase aligned clock signals for each memory device disposed on the module." *Id*. at 12:61-64. Therefore, a Skilled Artisan would have understood at the time of Perego's disclosure that Perego's clock circuit 570a-b is a "*phase-lock loop device*."

178. I note that Amidi also discloses a phase-lock loop device, such as PLL 606, which is coupled to the printed circuit board of Amidi. EX1036 (Amidi) at Fig. 6A. Amidi explains that the "signals sent to PLL 606 include CLK0, and

CLK0_N. PLL relays the CLK0 and CLK0_N signals to register 608 and memory devices 306." *Id*. at [0050], *see also* EX1032 (JEDEC 21-C) at 4.20.4-29 to -35 (showing PLL circuits coupled to circuit boards of memory modules). While Amidi used a PLL on a separate integrated circuit, Perego used a phase-lock loop device that is internal of its buffer circuit. I do not see this distinction to be relevant to the claim in light of the specification. EX1001 at 5:51-55 ("In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits"), 6:48-54 ("the logic element 40 comprises one or more integrated circuits"). To the extent such implementation details matter, both arrangements would have been obvious to a Skilled Artisan as evidenced by the disclosures of Perego and Amidi.

179. Thus, Perego discloses "*a phase-lock loop device coupled to the printed circuit board,*" as recited by Claim 16.

k) *[16.d.i]* the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

180. Perego discloses to a Skilled Artisan that "*the phase-lock loop device* [e.g., in the buffer device 405] *[is] operatively coupled to the plurality of DDR memory devices, the logic element, and the register*."

181. For example, as discussed above with reference to claim element **[16.c]**, **¶¶127-131**, Perego discloses that the buffer device includes the "*logic element*" and the "*register*." Perego also discloses that the buffer device includes memory device interfaces 520 which "receive and transmit to memory devices disposed on the module (e.g., see FIGS. 4A, 4B and 4C) via channels." EX1035 (Perego) at 11:48-51, Fig. 5B reproduced below, annotated).

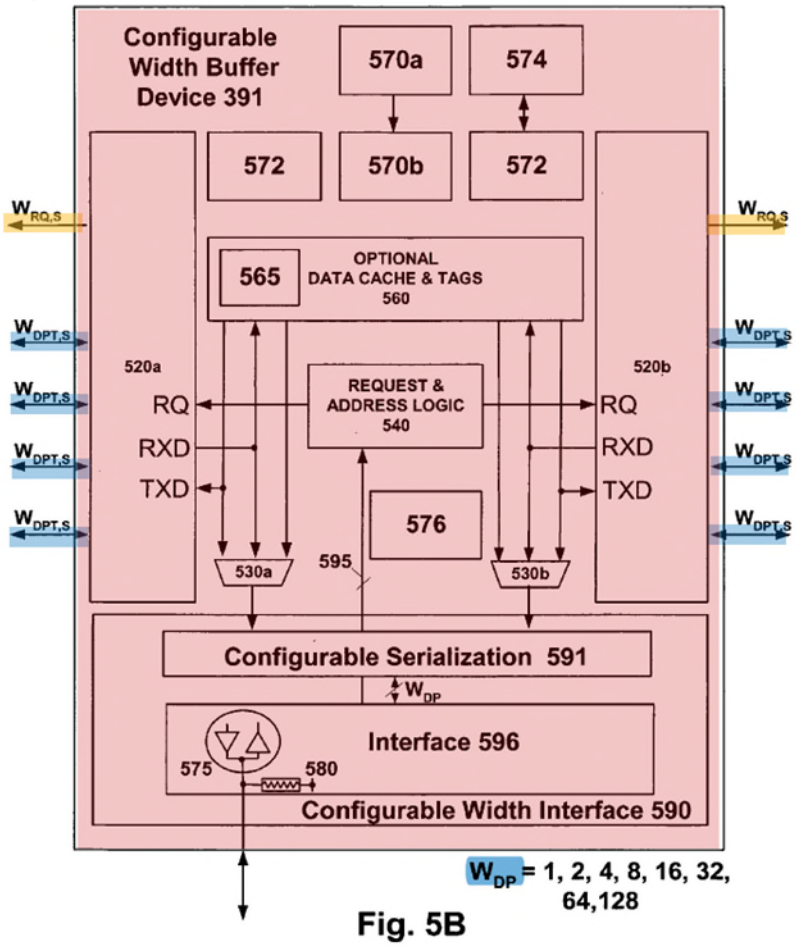


Fig. 5B

Perego further explains that in the buffer device, "clock circuit 570a–b includes one or more clock alignment circuits for phase or delay adjusting internal clock

signals with respect to an external clock (not shown). Clock alignment circuit may utilize an external clock from an existing clock generator, or an internal clock generator to provide an internal clock, to generate internal synchronizing clock signals having a predetermined temporal relationship." *Id.* at 12:65-13:5

182. A Skilled Artisan would have understood from Perego's disclosure that clock circuit 570a-b includes a "*phase-lock loop device*" that provides internal clock and synchronizing signals to the circuits within the buffer device. Thus, clock circuit 570a-b ("*phase-lock loop device*") is operatively coupled to the configurable width interface 590 (including the claimed "*register*"), request & address logic 540 (included in the claimed "*logic element*"), and the interfaces 520 which, in turn, are operatively coupled to "*the DDR memory devices*" in the implementation discussed above and shown below. *See* EX1035 (Perego) at FIG. 4B (reproduced below with the modifications for DDR SDRAMs as described by Perego).

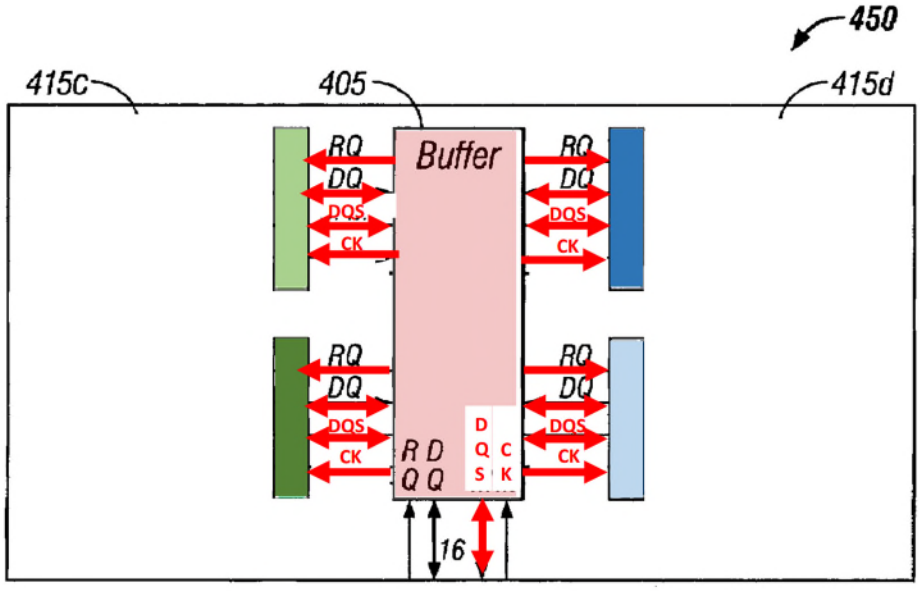


FIG. 4B

As illustrated here, the buffer 405 provides the clock signals to the DDR SDRAM x16 memory devices. Indeed, a Skilled Artisan would have understood that, in a DDR SDRAM module, the clock signals provided to the memory devices are generated by a "*phase-lock loop device*" (i.e., PLL) as confirmed by Amidi and the Skilled Artisan's knowledge. EX1036 (Amidi) at Fig. 6A; EX1032 (JEDEC 21-C) at 4.20.4-17.

183. I understand that Patent Owner has argued in the past that Amidi does not disclose that its PLL is coupled to the claimed "*logic element*." *See supra* ¶64. A Skilled Artisan, however, would have understood that a logic element which generates chip select signals for the memory devices needs to be in sync with the other signals, including the clock signal, received by the memory devices from the PLL. EX1029 (JESD79-2) at p.6 (explaining that "CK and CK are differential

clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK."). Accordingly, in both Perego and the combination of Perego and Amidi, a Skilled Artisan would have understood, and have been motivated to, operatively couple a "*logic element*," like Perego's request & address logic 540, to the clock generation circuitry 570a-b ("*phase-lock loop device*") that also provides clock signals for the memory devices.

184. Thus, Perego discloses to a Skilled Artisan that "*the phase-lock loop device [is] operatively coupled to the plurality of DDR memory devices, the logic element, and the register,*" as recited by Claim 16.

l) *[16.e]* wherein the command signal is transmitted to only one DDR memory device at a time.

185. Perego discloses "*wherein the command signal is transmitted to only one DDR memory device at a time*" for the reasons discussed above with reference to claim elements **[16.b.i], ¶¶118-126,** and **[16.c.iv], ¶¶ 169-175,** in an implementation like the one shown below where each memory device has a dedicated channel. EX1035 (Perego) at 10:17-21 ("It is conceivable that if each channel and memory device interface is made narrow enough, then a dedicated channel between each memory device and the buffer device may be implemented

on the module.") & FIG. 4B (reproduced below and modified according to the described implementation).

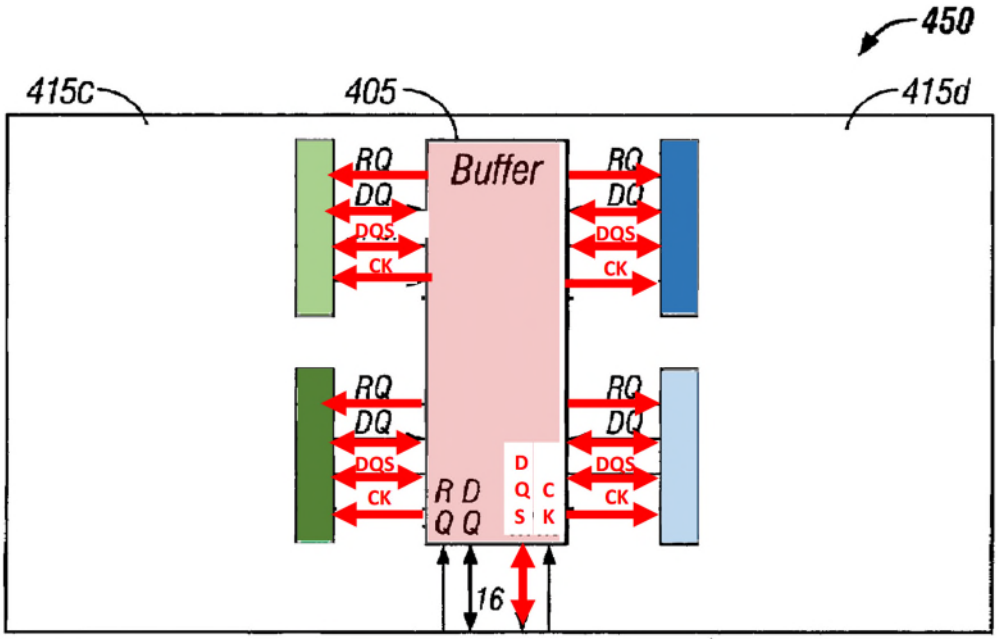


FIG. 4B

186. For example, Perego discloses that, "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370." EX1035 (Perego) at 6:15-19. Therefore, Perego expressly discloses selecting "one" memory device and transmitting the corresponding signals to the selected memory device. Perego also explains that, "[b]y accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is

higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks)." *Id.* at 15:31-45. A Skilled Artisan would have understood from this disclosure that the command signal is not transmitted to memory devices which do not participate in the data transaction (e.g., they do not receive the read or write command), consistent with the JEDEC standard, *supra* ¶¶73-77;EX1029,6,49. Thus, when the width of one memory device is the same as the width of the module (e.g., each rank has one x16 memory device), the command received at a given time is transmitted to only one DDR memory device at a time. In the case of a read command, for example, the read command is sent to only one memory device at a time so only that one memory device provides data in response to that read command.

187. Thus, Perego discloses "*wherein the command signal is transmitted to only one DDR memory device at a time*" as recited by Claim 16.

B. Ground 3: Claim 16 Is Rendered Obvious by Ellsberry

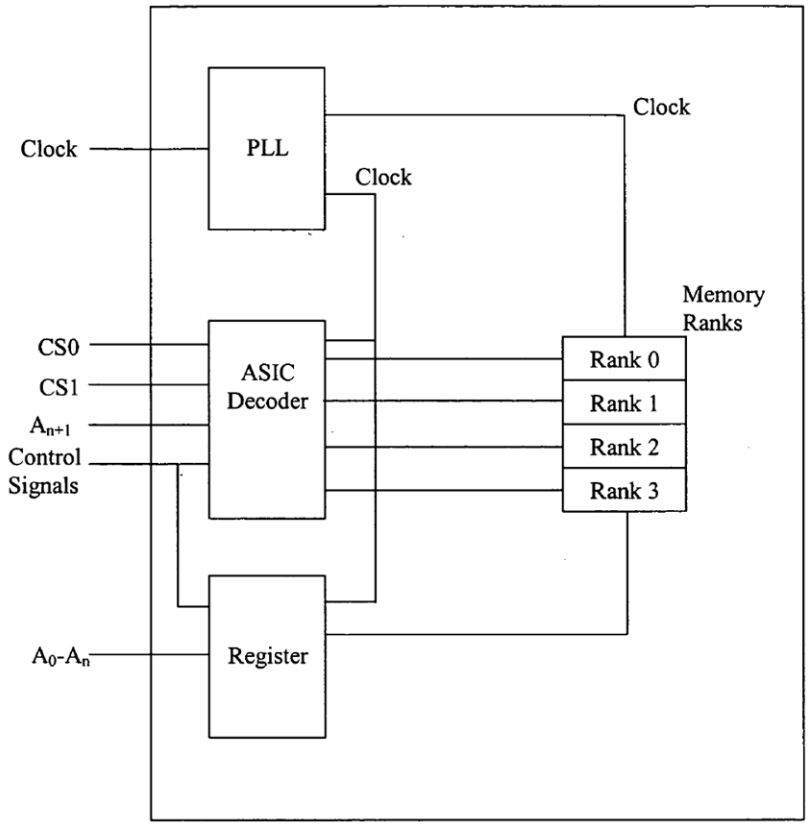
188. In my opinion, Ellsberry is prior art to, and renders obvious, claim 16 of the '912 Patent, as explained below.

1. Ellsberry is Prior Art to Claim 16 of the '912 Patent

189. I have reviewed the '668 provisional (the earliest priority application to the '912 Patent, filed March 5, 2004) (EX1006), and in my opinion a Skilled Artisan would have understood that it does not provide support for the full scope of

claim 16 of the '912 Patent. For example, the '668 provisional does not disclose the claimed "*logic element*" much less that such a "*logic element*" receives "*at least one row/column address signal, bank address signals, and at least one chip-select signal,*" as required by claim 16 of the '912 Patent. The next priority application — the '595 provisional filed on May 28, 2004 (EX1007) — is equally lacking. The '244 provisional filed on July 15, 2004 (EX1005) is the first priority application disclosing an ASIC Decoder, which as shown below includes some logic that a Skilled Artisan would have understood receives "*row/column address signal* [A_{n+1}]… *and at least one chip-select signal* [CS0 and CS1]." EX1005 at 10, Fig. 1 (reproduced below).

Figure 1:



The ’244 provisional, however, does not disclose that the ASIC Decoder receives any “*bank address*” signal as required by the “*logic element*” of claim 16 of the ’912 Patent. *Id*. In fact, the ’244 provisional does not even mention the words “*bank address*” anywhere, confirming that the applicants did not have possession at that time of all the requirements of claim 16 of the ’912 Patent. EX1005. Accordingly, a Skilled Artisan would have understood that none of the provisional applications (EX1005, EX1006, and EX1007) provides sufficient support for claim 16 of the ’912 Patent.

190. The next priority application of the '912 Patent was filed on March 7, 2005, and issued as U.S. Patent No. 7,286,436 (the '436 Patent). EX1009. In my opinion, a Skilled Artisan would have understood that the '436 Patent also fails to provide the requisite support for claim 16 of the '912 Patent. For example, the '436 Patent fails to disclose any embodiment including "*a circuit*" comprising "*a logic element*" and "*a register*" as required by claim 16 of the '912 Patent and as shown in Figure 1A of the '912 Patent with the labels 40 and 60, respectively. *See* EX1009 (e.g., none of the drawings illustrate any module including a logic element and a register).[2] The '436 Patent also does not include any Verilog code showing the use of the row address and/or bank address signals for rank multiplication (discussed above in ¶173), which was only added later as part of the continuation-in-part filed on July 1, 2005. I also note that the '436 Patent does not reference or claim priority to the '244 provisional filed on July 15, 2004. EX1009. Therefore, I have not seen any evidence that the inventors were in possession of

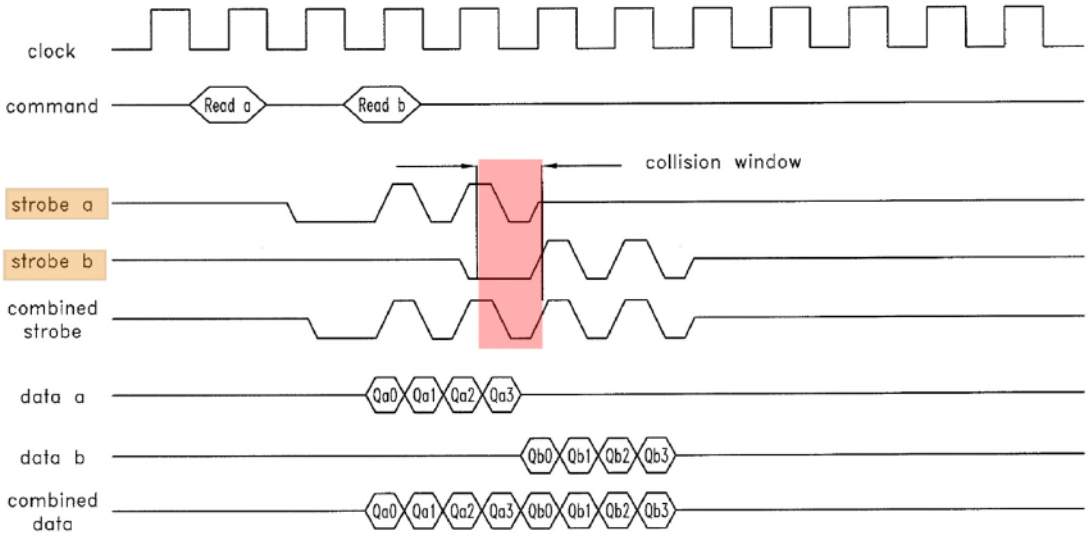
[2] I note that Figures 10A and 10B of the '436 Patent, in addition to lacking a "*register*," disclose that the module has the same number of ranks (two) as the number of chip selects (CS0, CS1) received from the system memory controller. Thus, the implementations of Figures 10A and 10B also lack the requirement in claim 16 of the '912 Patent that "*the second number of ranks [is] less than the first number of ranks.*"

any type of combination of the disclosure of the ’244 provisional and the ’436 Patent at the time of filing for the ’436 Patent on March 7, 2005.

191. For at least these reasons, in my opinion a Skilled Artisan would have understood that the inventors of the ’912 Patent were not in possession of the full scope of claim 16 of the ’912 Patent as of March 7, 2005 (or at any time before July 1, 2005), including the claimed selection based on “*bank address signals*” and the claimed “*circuit*” having a “*logic element*” and a “*register*.”

192. The next application in the priority chain was filed on July 1, 2005, as a continuation-in-part of the’436 Patent, and issued as the ’386 Patent. EX1008 at p.1. The subject matter added by the ’386 Patent includes recognition of the problem of “back-to-back adjacent read commands which cross memory device boundaries” in which case “the last data strobe of memory device ‘a’ collides with the pre-amble time interval of the data strobe of memory device ‘b,’ resulting in a ‘collision window.’” EX1001, 23:65-24:12 & FIG. 5; *see also* EX1008 (’386 Patent) 24:16-30 & FIG. 5 (reproduced below, annotated to highlight the collision, red, between strobes a and b, orange).

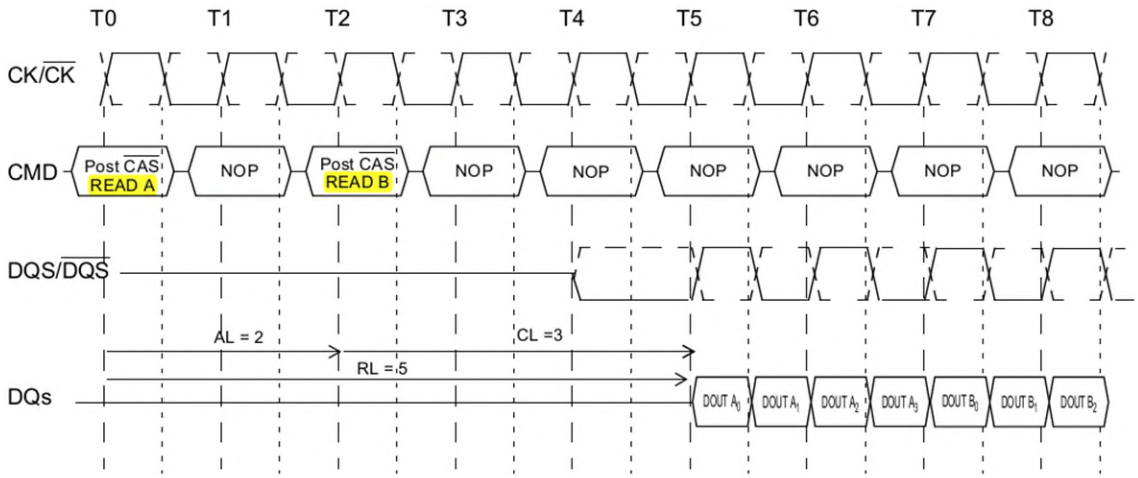
FIG. 5



As illustrated above in Fig. 5 of the '386 Patent, a Skilled Artisan would have understood that such a "collision" means that the two memory devices would try to drive the same signal line ("combined strobe") causing signal errors and potentially destroying the drivers in the memory devices. EX1043 (Stone) 89-90 ("A bus conflict can be more disastrous than portrayed here. For example, what happens when tri-state drivers engage in a bus conflict? In this case, there is a possibility of damaging the bus drivers because the conflict creates a low impedance path … The high current through this path can burn out both driving gates."). Neither the priority provisional applications nor the '436 Patent filed before July 1, 2005, addressed these collisions, and thus a Skilled Artisan would have understood from the '386 Patent that the disclosures in the earlier applications, i.e., before July 1,

2005, would not have worked in normal operation — and thus the inventors did not have possession of the full scope of claim 16 of the '912 Patent — because collisions could result during read operations, making the memory module unusable as a practical matter.

193. Indeed, a Skilled Artisan would have understood that back-to-back read commands were part of the JEDEC standards, and thus part of the normal operation of memory modules at the time. *See, e.g.*, EX1029 (JESD79-2) at p.28 (Fig. 27 reproduced below showing that, for DDR2 memories, "seamless burst read operation is supported by enabling a read command at every other clock for BL=4 operation"); *see also id*. at pp.28-29 (showing a read operation with a burst length of 8 interrupted by another read operation); *see also* EX1030 (JESD79) at p.19 (Fig. 8 showing consecutive reads with concatenated data bursts for DDR1 memories).



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

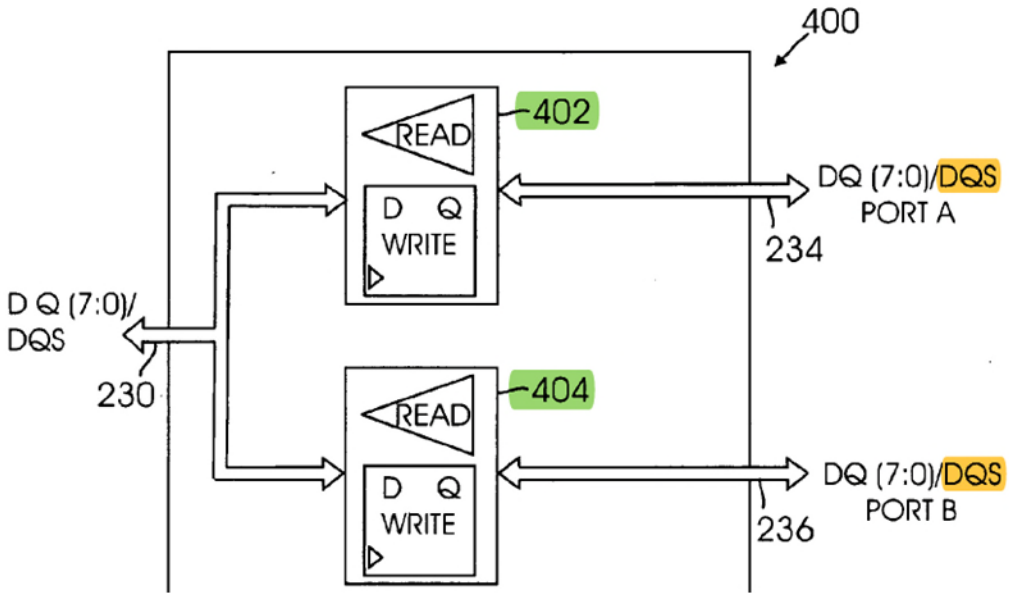
The ’436 Patent fails to mention the term “burst,” much less avoiding collisions of subsequent bursts of data strobe signals. Instead, the ’436 Patent mentions in general terms “sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks…,” without describing how to avoid collisions (e.g., by electrically isolating subsequent bursts of data strobes, as was later disclosed on July 1, 2005, as discussed below). EX1009, 18:3-6. Therefore, a memory module made according to the disclosure of the ’436 Patent and/or the prior provisional applications would fail, and could even “burn” the drivers of the memory devices, during standard back-to-back read operations.

194. The portions of the ’912 Patent added July 1, 2005, disclose a solution to the problems described above that existed with the ’436 Patent and the earlier

provisional applications: during back-to-back read operations, "collisions are avoided by a mechanism which *electrically isolates the DQS data strobe signal lines 104 of the memory devices from one another during the transition from the first read data burst* of one rank of memory devices *to the second read data burst* of another rank of memory devices." EX1001, 24:23-28 (emphasis added); EX1008 ('386 Patent), 24:41-56. The '912 Patent also discloses that "the appropriate components of the isolation device 120 are switched to enable and disable the DQS data strobe signal lines 104 to mitigate [] collisions." EX1001, 25:58-60; EX1008 ('386 Patent), 26:9-12. These solutions to the problem of back-to-back adjacent read commands were not disclosed in any of the applications before July 1, 2005. And the full scope of claim 16 of the '912 Patent encompasses back-to-back adjacent read commands with the solution disclosed above. For example, the '912 Patent's claim 16 requires selecting one or two ranks which a command signal is transmitted to, and nothing in the claim language excludes that such command is a back-to-back read command across device boundaries, which could create a collision or damage the memory devices without the solution that the inventors disclosed only on July 1, 2005. *See* EX1001 claim 16 ("*the circuit further responds to command signal and the set of input signals from the computer system by selecting one of two ranks of the first number of ranks*

and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks").

195. I further note that Ellsberry had already disclosed this solution to back-to-back read operations, since its memory bank switch has a separate port (Port A and Port B) for each of the two memory devices emulating a higher-capacity memory device. EX1037, e.g., at Fig. 4 (reproduced below in part, annotated).



During back-to-back read operations across memory devices, a first data strobe signal (DQS in bus 234) is received, e.g., by bidirectional driver 402 through Port A from a first memory device, and a second data strobe signal (DQS in bus 236) is received by bidirectional driver 404 through Port B from a second memory device, where the first and second memory devices are used to emulate a higher-capacity

memory device. EX1037,[0031],[0040],[0045]&FIG.4. Therefore, the strobe signals are separated by bidirectional drivers 402 and 404, so collisions of the DQS signals can be avoided. Indeed, as shown above, Ellsberry discloses that the two bidirectional drivers 402 and 404 are coupled to a system bus 230, including its own data strobe signal. Thus, Ellsberry discloses to a Skilled Artisan that data (DQ) and strobe (DQS) signals are driven to the system bus 230 only by one of the bidirectional drivers 402 and 404 in order to avoid bus conflicts. *See also* EX1043 (Stone) at pp.89-90 (explaining bus conflicts). This solution of selectively coupling by Ellsberry is similar to the solution that the '912 Patent later disclosed to the same problem. *See* EX1001 at 25:6-25 & Fig.6D (added July 1, 2005). An important difference, though, is that the '912 Patent uses FET switches for the selective coupling, EX1001 at 24:45-49, while Ellsberry explains that FET switches are too slow and imprecise to comply with the JEDEC standards, EX1037 at [0009]; *see also id.* at [0057] ("Field Effect Transistor (FET) based switches are too slow for the required high-speed switching as their switching speed is too imprecise."). Instead of FET switches, Ellsberry uses bidirectional drivers and, with the resulting "fast switching between memory banks[,] the switch and control architecture of the present invention permit memory access and distributed selection between memory devices at speeds not achievable in the prior art that complies with the standards for DDRI and DDRII." *Id*.

196. Therefore, a Skilled Artisan would have understood that, before July 1, 2005, the inventors of the '912 Patent were not in possession of, and did not provide an enabling disclosure for, the full scope of claim 16 of the '912 Patent.

2. Claim 16 is Unpatentable

a) *[16.pre] A memory module connectable to a computer system, the memory module comprising:*

197. To the extent the preamble is limiting, Ellsberry discloses a "*memory module connectable to a computer system*."

198. Ellsberry discloses a memory module, such as memory module 106 with a capacity expanding device 108, that is connectable to a computer system, such as computing system 100 including a processing unit 102 and I/O controller 104. EX1037 at [0027], Fig. 1 (reproduced below).

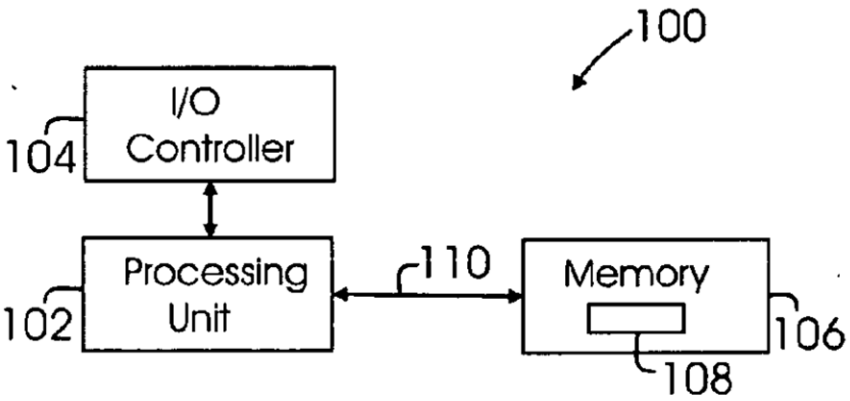


Fig. 1

199. For example, Ellsberry discloses that "[t]he term 'memory module' refers to any package in which one or more memory devices are mounted (e.g., DIMM, SIMM, etc.)." EX1037 at [0023]. Ellsberry further explains that:

> FIG. 1 illustrates a computing system 100 that includes a capacity-expanding memory device according to one embodiment of the invention. The computing system 100 may include a processing unit 102 coupled to an input/output (I/O) controller 104 to receive and/or send information. The processing unit 102 may also be coupled to a memory module 106 to retain or store information. The memory module 106 may include an embodiment of the capacity-expanding memory device 108 that permits increasing the memory capacity without increasing the bus size or communication path 110 to and/or from the memory module 106. In one implementation of the invention, the bus size or communication path 110 to and/or from the memory module 106 is not modified to accommodate the capacity-expanding memory device 108. Thus, the capacity-expanding memory device 108 is compatible with existing system architectures and transparent to the rest of the system (e.g., microprocessor, operating system, etc.). Moreover, the resistive and/or capacitive load on the bus 110 is not increased because the memory module 106 presents a single load to the bus 110, not the load of the individual memory devices coupled thereto.

EX1037 at [0027].

200. An implementation of Ellsberry's memory module is shown in more detail, e.g., in Fig. 12. EX1037 at [0052] ("FIGS. 10, 11, 12 and 13 illustrate different configurations of memory modules (e.g., DIMMs) that can be built using combinations of the control unit and bank switch according to various embodiments of the invention. These configurations employ the control unit and bank switch previously described."), Fig. 12 (reproduced below with annotations).

In particular, Ellsberry explains that "FIG. 12 illustrates a single chip-select memory configuration in which one control unit 1202 [(red)] and one bank switch 1204 [(blue)] are used to control two memory banks 1206 [(light blue box)] &1208 [(light green box)], each memory bank having one memory device 1210." *Id.* at [0055].

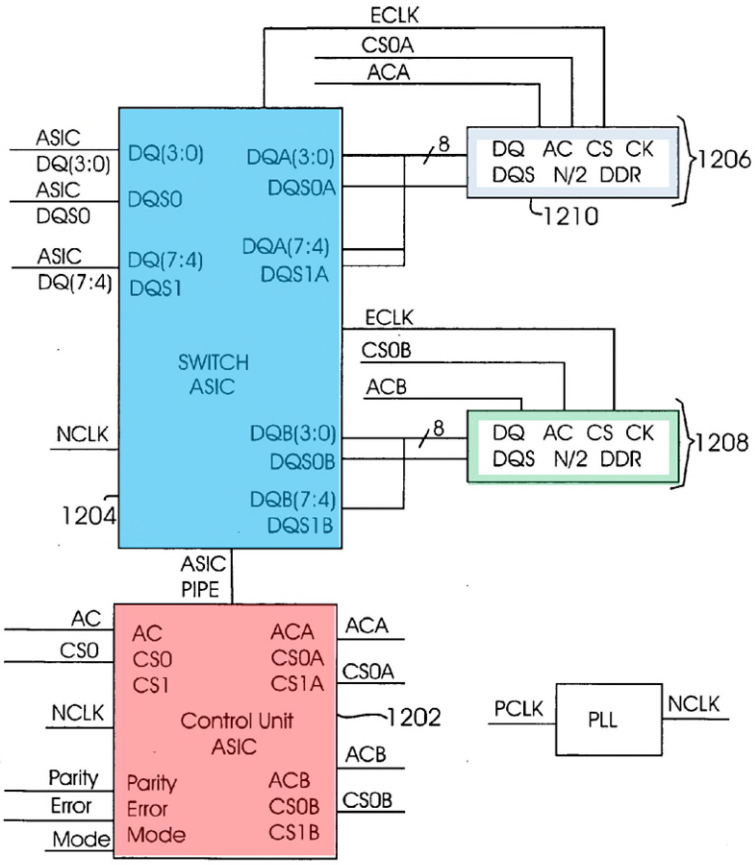


Fig. 12

201. I note that my analysis here focuses on Ellsberry's implementation in Fig. 12 for the sake of clarity, since it has only two memory devices (and two ranks, identified by chip-select signals CS0A and CS0B). Ellsberry also discloses

other implementations which have more memory devices (and ranks), such as Fig. 13 illustrating an embodiment with four memory devices (and four ranks, identified by CS0A, CS1A, CS0B, and CS1B). EX1037 at Fig. 13 (reproduced below, annotated). My analysis below applies equally to this implementation.

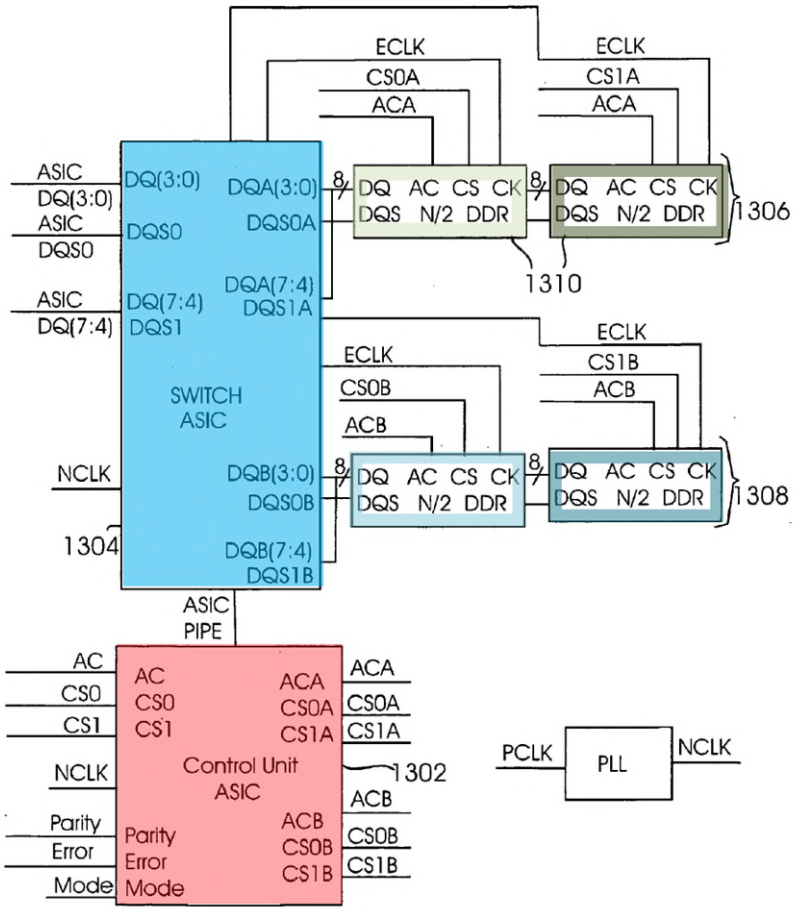


Fig. 13

202. I also note that the Board has previously determined, in a Final Written Decision against Netlist, that Ellsberry discloses "*[a] memory module . . . configured to communicate with a memory controller*" wherein the memory module includes a "*printed circuit board (PCB) having an edge connector*

positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket," which encompasses the requirements of [16.pre] and thus provides further support for the conclusion that Ellsberry discloses [16.pre]. EX1038 at 17, 23-25.

203. Thus, Ellsberry discloses "*a memory module connectable to a computer system*" as recited by Claim 16.

b) *[16.a] a printed circuit board*

204. Ellsberry discloses to a Skilled Artisan that its memory module includes "*a printed circuit board*."

205. For example, Ellsberry discloses that, "[t]ypically, memory modules include a small ***circuit board*** with contact pads along one edge to couple to a slot on another circuit board, such as a computer motherboard. In some cases, the contact pads are placed on two surfaces of the small circuit board along an edge of the small circuit board. In some implementations, the number and size of the contact pads may be defined by various bus or communication standards. In other implementations, the physical space available for such contact pads and/or electrical traces or buses may determine the number and size of the contact pads." EX1037 at [0002] (emphasis added).

206. A Skilled Artisan would have understood — and at least would have found it obvious — at the time from Ellsberry's disclosure that Ellsberry's "circuit board" is a printed circuit board (PCB). For example, Ellsberry discloses that the DDR2 memory devices have a "FBGA" (Fine-Pitch Ball Grid Array) package which a Skilled Artisan would have understood is designed for mounting the memory devices on a PCB. EX1037 at Fig. 5, *see also* EX1032 (JEDEC21-C) at 4.20.4-22, -66 (showing "BGA" as a package compatible for mounting on DIMM memory modules, which have a "printed circuit board design"); EX1029 at pp.1-5 (describing MO-207 packages for DDR2 memory chips with specific solder ball patterns). Indeed, using printed circuit boards was common for memory modules at the time. *See, e.g.*, EX1035 (Perego) at 5:60-62 ("memory subsystems are incorporated onto individual substrates (e.g., PCBs)"); EX1032 at 4.20.4-29 ("Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals.").

207. I also note that the Board has previously determined, in a Final Written Decision against Netlist, that Ellsberry discloses a memory module with a "*printed circuit board (PCB),*" which encompasses the requirements of [16.a] and thus provides further support for the conclusion that Ellsberry discloses [16.a]. EX1038 at 23-24.

208. Thus, Ellsberry discloses and renders obvious to a Skilled Artisan "*a printed circuit board*" as recited by Claim 16.

c) *[16.b] the* plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,

209. Ellsberry discloses to a Skilled Artisan that its memory module includes "*a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board*."

210. For example, Ellsberry discloses that "[t]he term 'memory module' refers to any package in which one or more memory devices are mounted (e.g., DIMM, SIMM, etc.)." EX1037 at [0023]. As discussed above with reference to claim element **[16.a], ¶¶204-208**, Ellsberry discloses that such a package includes a circuit board which a Skilled Artisan would have understood can be a printed circuit board. Ellsberry also discloses that the "[m]emory devices are typically mounted on one or two surfaces of the small circuit board of the memory module. Dynamic random access memory (DRAM) chips are often used in memory module applications. The memory devices are communicatively coupled to the contact pads such that data may be sent to a memory module and stored in the memory devices. Various electrical paths are used to transfer data, specify a memory address, and control the flow of the data to and from the memory devices." EX1037 at [0003].

211. Ellsberry also specifically teaches that its "invention permits two separate SDRAM DDR devices to appear as a single higher-capacity SDRAM DDR device to a source device (e.g., microprocessor, memory controller, etc.)." EX1037 at [0026]. In particular, "[i]n various embodiments of the invention, the control unit and bank switch combination may support SDRAM DDR1 and DDR2 specifications (incorporated herein by reference) with memory capacities of 256 Mb, 512 Mb, and 1 Gb in speed grades of 200/266/333/400 Mbps in DDR1 and capacities of 256 Mb, 512 Mb, 1 Gb, and 2 Gb in speed grades of 400/533 Mbps in DDR2." EX1037 at [0046].

212. I also note that the Board has previously determined, in a Final Written Decision against Netlist, that Ellsberry discloses a memory module with "*memory devices*" on a "*printed circuit board (PCB),*" where the memory devices are shown as "DDR2" memory devices, which encompasses the requirements of [16.b] and thus provides further support for the conclusion that Ellsberry discloses [16.b]. EX1038 at 4, 23-26.

213. Thus, Ellsberry discloses "*the plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,*" as recited by Claim 16.

d) *[16.b.i]* the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

214. Ellsberry discloses "*the plurality of DDR memory devices having a first number of DDR memory devices* [e.g., two x8 memory devices] *arranged in a first number of ranks* [e.g., two ranks]."

215. For example, Ellsberry discloses that, in one implementation, its module has two x8 DDR memory devices arranged in two ranks (called memory banks 1206 &1208 corresponding to ports A and B, respectively) indicated by chip-select signals CS0A and CS0B as shown in FIG. 12 of Ellsberry. EX1037 at Fig. 12 (reproduced below, annotated).

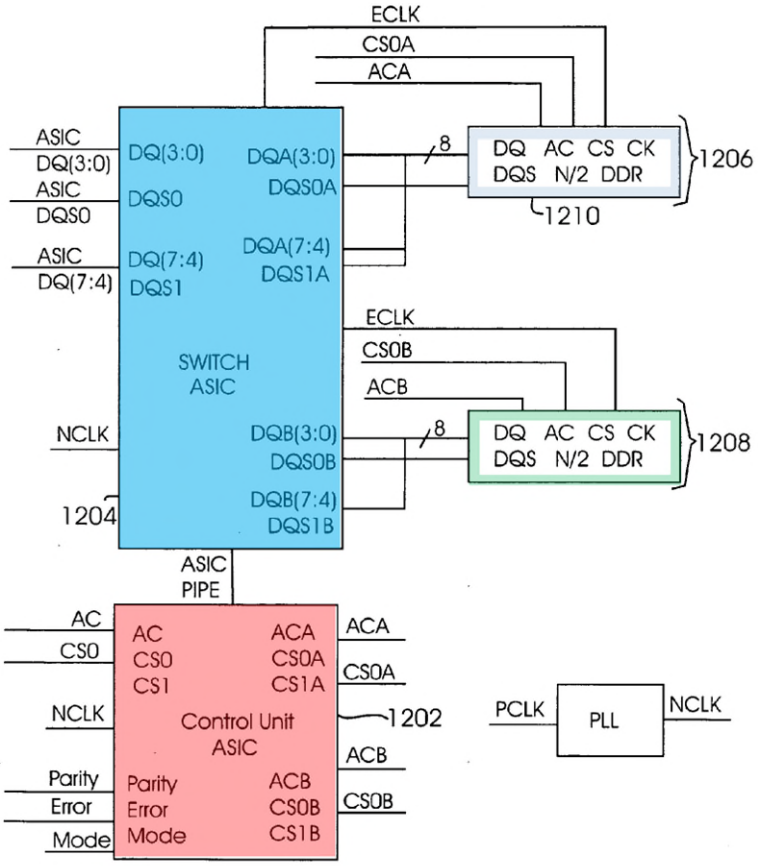


Fig. 12

216. As shown in Fig. 12, Ellsberry discloses that each memory device has its own separate chip select signal (CS0A, CS0B) and each memory device has the same data width of 8 bits ("/8") as the module with a single data buffer (blue, coupled to eight system data lines DQ[7:4] and DQ[3:0]). EX1037 at Fig. 12 (reproduced above, annotated). Therefore, Ellsberry discloses a memory module which is eight bits wide and has two 8-bit wide ranks (light blue, and light green, above), each controlled by a separate chip select signal (CS0A, CS0B, above). For the same reasons, Ellsberry discloses that the module shown in the implementation

of Fig. 13 is also eight bits wide and has four 8-bit wide memory devices arranged in four 8-bit wide ranks, each controlled by a separate chip select signal (CS0A, CS1A, CS0B, CS1B).

217. Indeed, Ellsberry discloses to a Skilled Artisan that a memory module can include only a single data group having a data buffer and corresponding memory devices. EX1037 at [0021] ("FIGS. 10, 11, 12 and 13 illustrate different configurations of memory modules (e.g., DIMMs) that can be built using combinations of the control unit and bank switch according to various embodiments of the invention."). Ellsberry explains that the operation of one data group, as shown in Figs. 12 and 13, "is ***expanded when*** implementing a wider memory bus formed by ***several data groups*** composed of a plurality of memory bank switches and the associated memories." *Id*. at [0035]. Thus, Ellsberry discloses to a Skilled Artisan that the configuration can, but is not required to, be expanded to several data groups. *See also*, *e.g.*, EX1035 (Perego), e.g., at Fig. 5B (disclosing that the data width W_{DP} of a memory module can be 8-bit wide).

218. To the extent one might argue that Ellsberry discloses only memory modules with multiple data buffers, it would have been obvious to a Skilled Artisan to make a memory module which has only a single data group as expressly shown in Ellsberry's FIGS. 10-13. Indeed, Ellsberry teaches that only a wider memory bus would require several data groups. EX1037 at [0035]. Thus, for a

system where the data bus is only 8 bits wide, a Skilled Artisan would have been motivated to have only a single data group as taught by Ellsberry. A Skilled Artisan would have understood that such a single data group would have been simpler to make and required fewer parts, thus having fewer error sources, than the module with multiple data groups.

219. Furthermore, the '912 Patent itself supports that a "rank" could include a single memory chip, as discussed above, *supra* ¶¶73-77 (construing "rank"). For example, the '912 Patent discloses that:

> [t]he DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. … The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. … During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals.

EX1001 at 2:16-42. A Skilled Artisan would have understood at the time that this description of "rank" in the '912 Patent would be satisfied by a single memory device whose data width is the same as the data width of the memory module.

220. In addition, the '912 Patent explains that, "[i]n certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one

memory device at a time." EX1001 at 8:50-54. A Skilled Artisan would have understood from this disclosure that, "[i]n such embodiments," each rank has only one memory device, because "the command signal[, e.g., read,] is passed to the selected rank only," and this command signal "is sent to only one memory device."

221. Ellsberry's disclosure is also consistent with the understanding of a Skilled Artisan that a memory module can have a single rank and in that rank there can be a single memory device. EX1033 at 413 ("Essentially, a *rank* of memory is a '*bank*' of ***one or more*** DRAM devices that operate in lockstep in response to a given command," emphases in bold italics added); EX1037 (Ellsberry) at [0023] ("The term "memory module" refers to any package in which ***one or more*** memory devices are mounted (e.g., DIMM, SIMM, etc.)."); *see also supra* ¶201 (discussing Fig. 13 of Ellsberry as an alternative implementation of a four rank module responding to control signals directed to a two-rank module).

222. I also note that the Board has previously determined, in a Final Written Decision against Netlist, that Ellsberry discloses *"a plurality of memory devices,"* EX1038 at 19 (citing EX1037 (Ellsberry) at [0003], [0026], [0030], and [0032]), where those memory devices are organized in "ranks" as properly construed here (i.e., an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module), *see supra*

¶¶73-77. In particular, the Board pointed to "four memory banks (i.e., Bank 0, Bank 1, Bank 2, and Bank 3)" corresponding to data groups, EX1038 at 19, and found that each of Ellsberry's multiple (*M*) data groups simultaneously output or receive one byte (*n*=8 bits), thus acting on the full bit width ($N=M\times n$) of the module. *Id*. at 17, 19-21 (citing EX1037 (Ellsberry) at [0031], [0040], Fig. 2). Accordingly, the Board found that each of Ellsberry's Bank 0, Bank 1, Bank 2 and Bank 3 discloses a respective "*rank*" as understood by a Skilled Artisan. These findings by the Board encompass the requirements of [16.b.i] and thus provide further support for the conclusion that Ellsberry discloses [16.b.i].

223. Thus, Ellsberry discloses "*the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;*" as recited by Claim 16.

e) *[16.c] a* circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,

224. Ellsberry discloses "*a circuit* [(e.g., Control Unit ASIC, red)] *coupled to the printed circuit board, the circuit comprising a logic element* [(e.g., control block)] *and a register* [(e.g., register 302)]," as illustrated in Figure 3 (reproduced and annotated below).

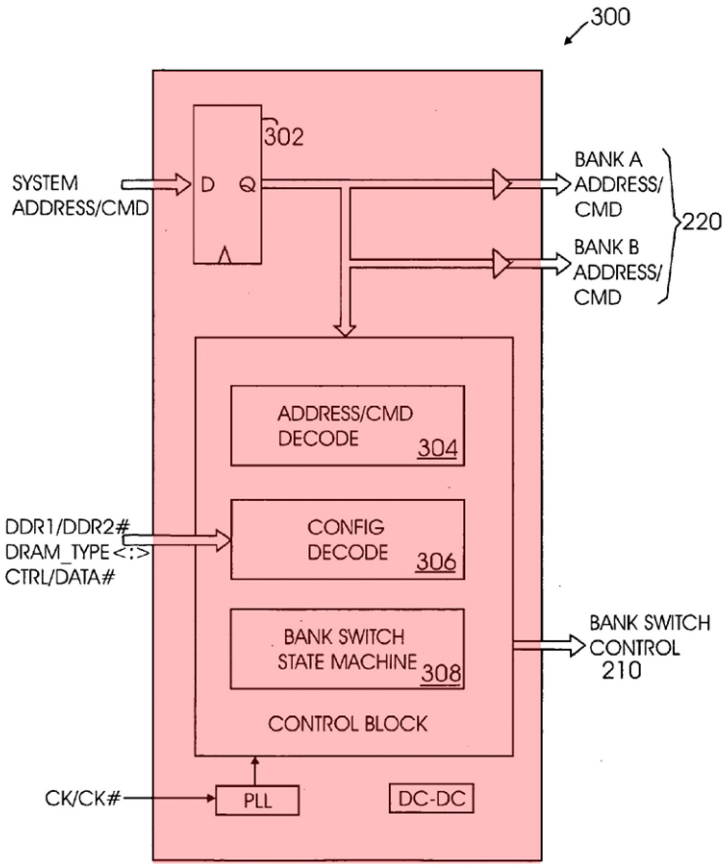


Fig. 3

For example, Ellsberry explains that "[m]emory addresses and command information are received from the DIMM interface 202, buffered in a register 302 … The memory address and command information is also decoded 304 … A bank switch state machine 308 then determines which memory bank should be activated or accessed." EX1037 at [0039]. A Skilled Artisan would have understood from this disclosure that the control block shown above in Figure 3 includes a "*logic element*" and "*register*" as required claim 16 of the '912 Patent.

225. Ellsberry also discloses that the control unit (red, above) is coupled to the circuit board of the memory module. EX1037 at [0047], [0049] ("A memory controller 510 is mounted on the substrate 502 and configured to control write and read operations to/from the memory devices 506. … According to one embodiment of the invention, a memory controller 510 is a control unit 204"); *see also id.* [0039] (explaining control unit 204 can include address and command processing system 300 in Fig.3). Therefore, a Skilled Artisan would have understood that the "*circuit*" of Fig. 3 of Ellsberry can be implemented as part of the Control Unit (red, below) in the implementation of Fig. 12 (and in Fig. 13 in the case of four ranks). EX1037,[0052].

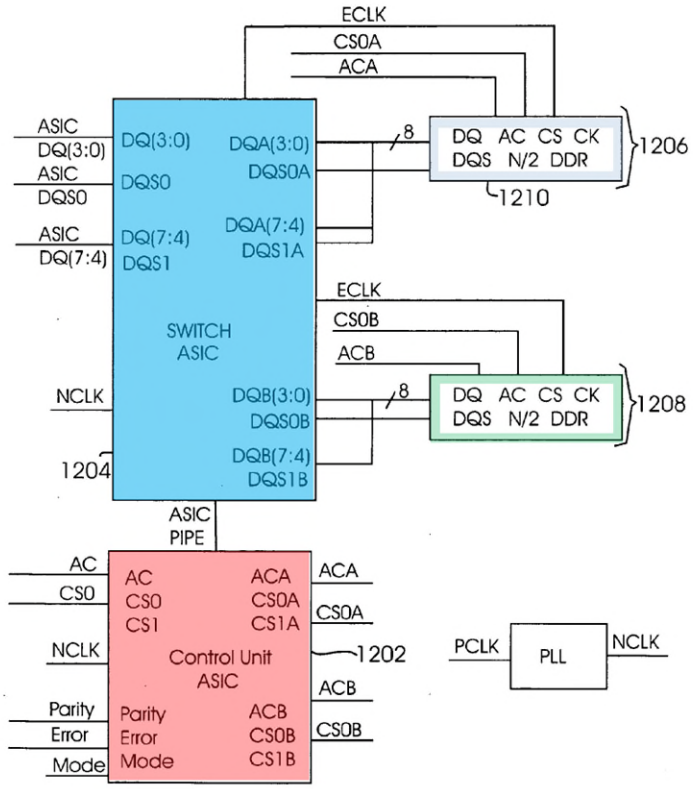


Fig. 12

226. I also note that the Board has previously determined, in a Final Written Decision against Netlist, that Ellsberry discloses *"a module control circuit . . . to produce first module control signals,"* EX1038 at 18-19, where those signals are identified as "registered" signals, *see* EX1037 (Ellsberry) at Fig.2, bus 220. These findings by the Board encompass the requirements in [16.c] of a "*circuit*" comprising a "*logic element*" (e.g., to generate first module control signals) and "*register*" (e.g., to output "registered" signals) and thus provide further support for the conclusion that Ellsberry discloses [16.c]

227. Thus, Ellsberry discloses "*a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,*" as recited by Claim 16.

f) *[16.c.i]* the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,

228. Ellsberry discloses "*the logic element* [e.g., the Control Block in Control ASIC (red)] *receiving a set of input signals from the computer system* [e.g., signals associated with a read or write command per the JEDEC standard, EX1029,6,49], *the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal* [per the JEDEC standard for DDR memory devices, EX1029,6,49&n.2 (A0-A15[3],BA0-BA2,CS)]." *See, e.g.*, EX1037 at FIG. 3 (reproduced below left, annotated, showing the registered system address/CMD signals received by the Control Block in the Control ASIC, red) & FIG. 12 (reproduced below right, annotated, showing the Control ASIC, red, receiving input address and command signals AC with input chip select signal CS0 separately shown).

[3] A10 is used for a command signal, rather than an address signal, for certain commands, such as Precharge, Write, and Read. EX1029,6,7-8,33-34,37,49.

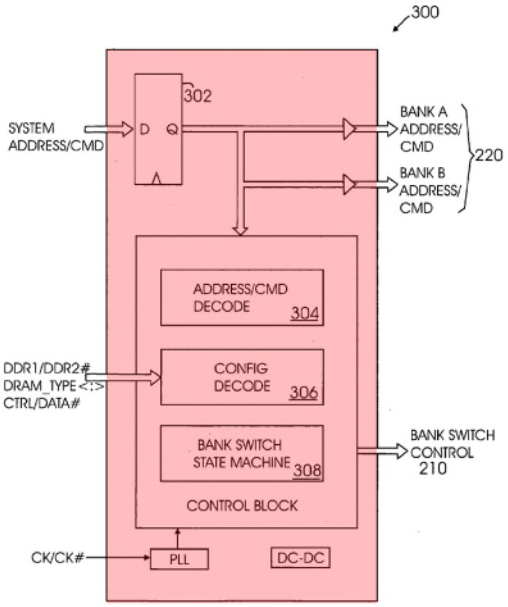


Fig. 3

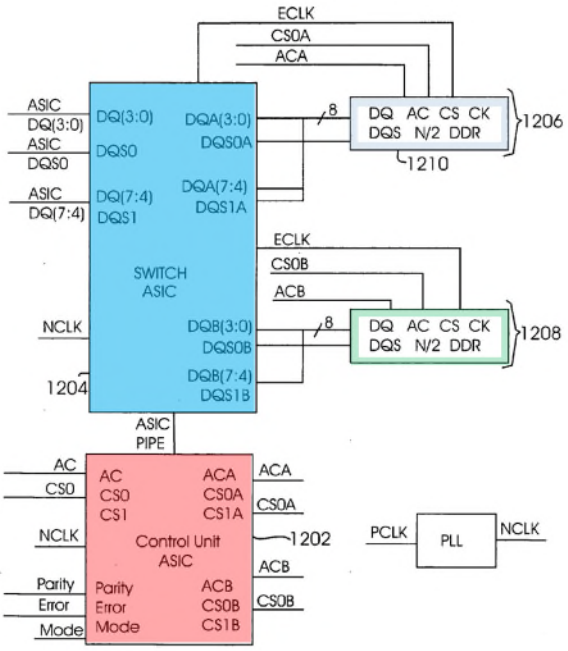


Fig. 12

Ellsberry also discloses that, for DDR SDRAM, a "command consists of RAS_n, CAS_n CS, WE_n, and A(10)." *Id*. at FIG. 8B, n.3 (reproduced below).

3. A command consists of RAS_n, CAS_n, CS, WE_n, and A(10).

Thus, a Skilled Artisan would have understood that the received address and command signals include "*row/column address*" signals (in Address/Command, "AC," signals), "*bank address*" signals (in Address/Command, "AC," signals to determine the target bank within each memory device for the read or write command), and a "*chip-select*" signal (CS, needed to select the rank of memory device(s) for the read or write command) for DDR SDRAMs. *Id.*; EX1029 (JESD79-2) at p. 6 (disclosing DDR2 memory chip input/output functions, reproduced below, annotated).

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$) (UDQS), ($\overline{UDQS}$) (LDQS), ($\overline{LDQS}$) (RDQS), ($\overline{RDQS}$)	Input/Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$, and $\overline{RDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.

See also id. at 49 & n.2 (reproduced below in part, explaining that row address is sent with a Bank Activate command, and column address is sent with Read and Write commands for a specific bank, as identified by bank address signals BA).

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

229. Furthermore, Ellsberry expressly discloses that the bank switch state machine 308 in the control unit ASIC uses the received bank address signals, including Bank A(2) (purple, below), to map the primary (input) address space of a simulated DDR2 memory device (e.g., red box, below) to the address space of two actual DDR2 memory devices on the module (e.g., blue and green boxes, below). EX1037 at [0039] ("For example, the state machine 308 may be the address mapping table illustrated in FIGS. 7A-F."), FIG. 7D (reproduced below, annotated, and with header information added from FIG. 7A).

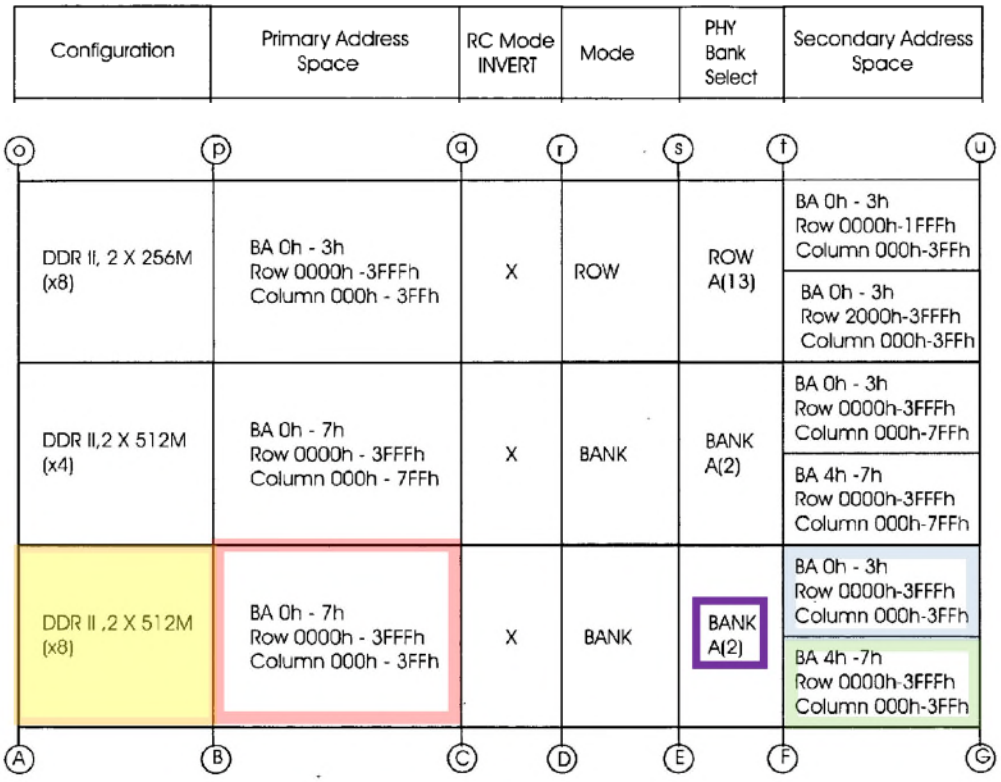


Fig. 7D

For example, as illustrated above, the state machine 308 selects the physical bank which is the target of a read or write operation based on bank address signals, including Bank A(2) for the case when two DDR2 512Mb eight-bit wide (x8) memory devices, one in each rank, emulates one DDR2 1Gb eight-bit wide (x8) memory device. *Id*. at [0037], *see also supra* ¶142 (citing EX1029 (JESD79-2) at p.7) (showing that the difference between 512Mb (blue) and 1Gb (red) addressing is bank address BA(2) for x8 memory devices).

230. As another example (illustrated below), a module can have two DDR2 256Mb eight-bit wide (x8) memory devices, one in each rank, to emulate one

DDR2 512Mb eight-bit wide (x8) memory device. EX1037 at [0037], Fig. 7 (reproduced below in part, annotated). In that case, the row address bit A(13) is used for the selection. *Id.*; *see also* EX1029 (JESD79-2) at p.7 (showing that the difference between 256Mb and 512Gb addressing is row address A_{13} for x8 memory devices).

Configuration	Primary Address Space	RC Mode INVERT	Mode	PHY Bank Select	Secondary Address Space
DDR II, 2 X 256M (x8)	BA 0h - 3h Row 0000h -3FFFh Column 000h - 3FFh	X	ROW	ROW A(13)	BA 0h - 3h Row 0000h-1FFFh Column 000h-3FFh BA 0h - 3h Row 2000h-3FFFh Column 000h-3FFh
DDR II,2 X 512M (x4)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 7FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-7FFh BA 4h -7h Row 0000h-3FFFh Column 000h-7FFh
DDR II ,2 X 512M (x8)	BA 0h - 7h Row 0000h - 3FFFh Column 000h - 3FFh	X	BANK	BANK A(2)	BA 0h - 3h Row 0000h-3FFFh Column 000h-3FFh BA 4h -7h Row 0000h-3FFFh Column 000h-3FFh

Fig. 7D

As shown in Figure 7 of Ellsberry (including the portion above), the mapping from the Primary to the Secondary Address Space also receives the bank address signals (BA) of the "Primary Address Space" used by the system memory controller. Furthermore, for the reasons discussed above with reference to Amidi, *supra*

¶¶158-163, a Skilled Artisan would have understood that the row address bit A(13) is bank specific and arrives before the read or write command, so Ellsberry's logic would use the bank address signals (BA) to properly store and retrieve the respective row address bit A(13) for each activated bank.

231. Thus, Ellsberry discloses "*the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,*" as recited by Claim 16.

g) *[16.c.ii]* the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,

232. Ellsberry discloses that "*the set of input signals* [(including AC and CS0, orange below)] *configured to control a second number of DDR memory devices* [e.g., the input signals are for one x8 DDR2 memory device] *arranged in a second number of ranks* [e.g., the input signals are for one rank], *the second number of DDR memory devices* [e.g., one] *smaller than the first number of DDR memory devices* [e.g., two x8 DDR2 memory devices] *and the second number of ranks* [e.g., one] *less than the first number of ranks* [e.g., two ranks]." EX1037, e.g., at Fig. 12 (reproduced below, annotated).

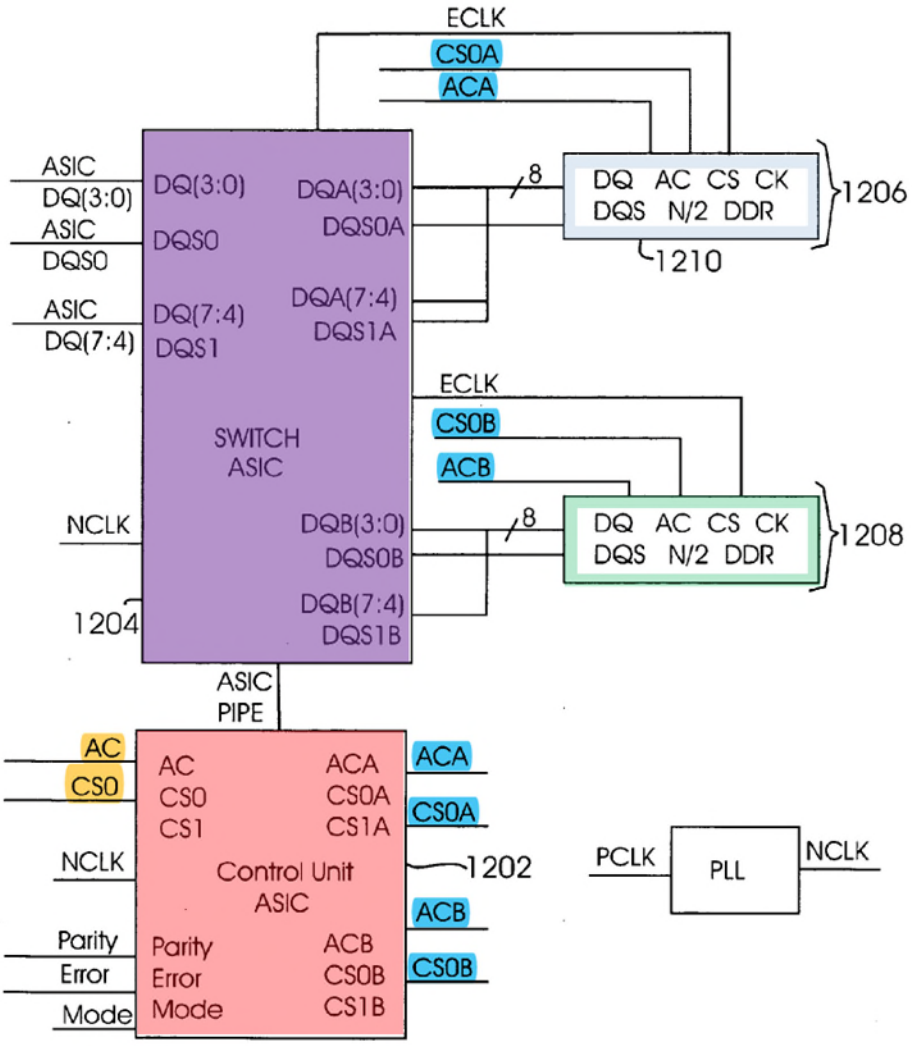


Fig. 12

See also Fig. 13 (showing another implementation where the input signals, including address and command signals AC and chip select signals CS0 and CS1, correspond to two ranks with one x8 memory device in each rank as seen by the system memory controller, while the module includes four ranks with one x8 memory device in each rank).

233. For example, Ellsberry discloses that, in one implementation, the primary address space (included in the "*set of input signals*") corresponds to a single x8 DDR2 memory device with 1Gb (2 times 512Mb) capacity (red, below), and the memory module uses two x8 DDR2 memory devices (yellow box, below), each having a 512Mb capacity (light green and blue, below) to simulate the larger capacity memory device. EX1037 at FIG. 7D (reproduced below, annotated, and with header information added from FIG. 7A).

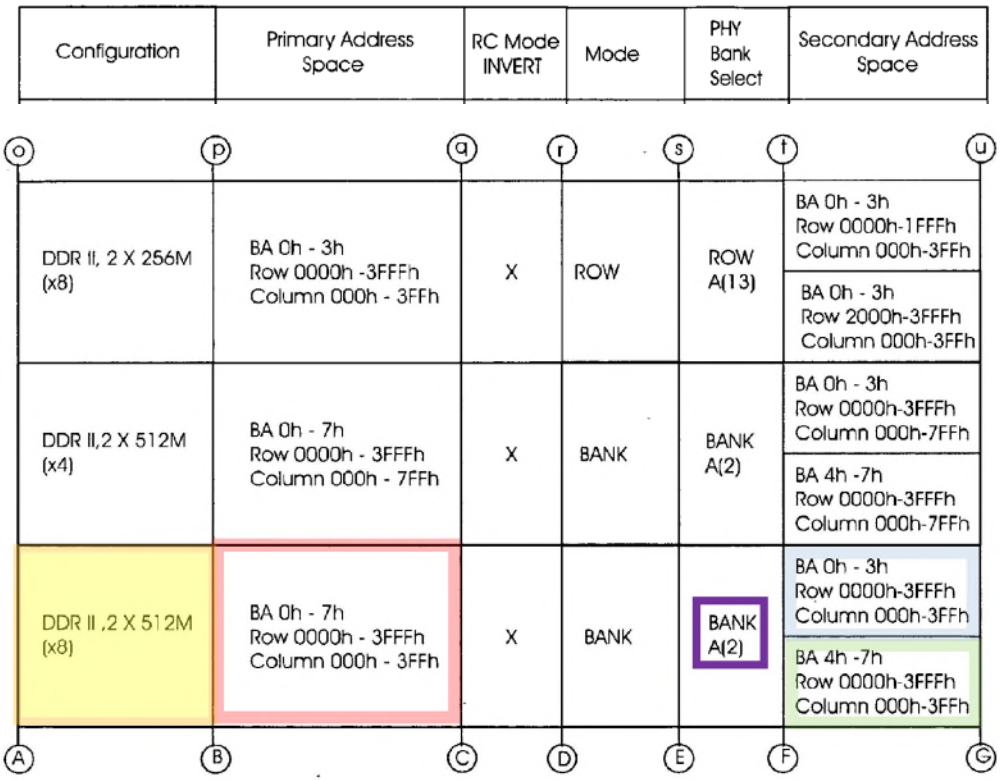


Fig. 7D

234. A Skilled Artisan at the time would have understood from this disclosure that the primary address space (red, above) shown in the highlighted

row of FIG. 7D corresponds to a JEDEC 8-bit wide (x8) memory device with a total capacity of 128MB (1Gb), and the secondary address space (light green and blue) corresponds to two JEDEC 8-bit wide (x8) memory devices, each with a capacity of 64MB (512Mb). EX1029 (JESD79-2) at 7 (Tables 2 and 3, reproduced below with annotations). Indeed, Ellsberry shows that the primary address space uses three bank address bits (BA 0h-7h, corresponding to BA0-BA2 in the standard below), 14 row address bits (Row 0000h-3FFFh, corresponding to A_0-A_{13} in the standard below) and 10 column address bits (Column 000h—3FFh, corresponding to A_0-A_9 in the standard below) as shown for a 128Mbx8 DDR2 memory device (red) by the JEDEC standard. *Id.*

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

235. Similarly, Ellsberry shows that the secondary address space uses two bank address bits (BA 0h-3h for the first device and BA 4h-7h for the second

device, corresponding to BA0, BA1 in the standard above), 14 row address bits (Row 0000h-3FFFh, corresponding to A_0-A_{13} in the standard above) and 10 column address bits (Column 000h—3FFh, corresponding to A_0-A_9 in the standard above) as shown for a 64Mbx8 DDR2 memory device (light blue and green) by the JEDEC standard. EX1037 at Fig. 7 (reproduced above). As also disclosed by Ellsberry, the difference in the address spaces is a bank address bit, Bank A(2) (i.e., BA2 in terms of the standard), which is used to select one of the two physical ranks on the module for a given address in the primary address space. This shows that Ellsberry uses the three bank address signals (BA) in the JEDEC standard to determine which rank of memory devices to select.

236. Importantly, this specific implementation of Ellsberry discloses an address mapping that is nearly identical to the "EXAMPLE 1" Verilog code in the '912 Patent describing 512Mb to 1Gb density multiplication with the transition bit being the bank address bit BA2. EX1001 at 14:17-23 ("An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA2 density transition bit is listed below in Example 1."). In EXAMPLE 1 of the '912 Patent, the Verilog code simply follows the JEDEC standard to identify different commands, including those related to pre-charge operations as conveyed by the pre-charge signal on line

A10 (blue). *Id.* at col. 14. In particular, the value a10_in (blue) is used to differentiate precharging all banks or a single bank. *Id.*

```
// Gated Chip Selects
assign      pcs0a_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,md reg set
            | (~rs0_in_N & ras_in_N & cas_in_N)                                    // ref exit, pwr dn
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)               // pchg all
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)// pchg single bnk
            | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ~ba2_in)          // activate
            | (~rs0_in_N & ras_in_N & ~cas_in_N           & ~ba2_in)               // xfr
            ;
assign      pcs0b_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,md reg set
            | (~rs0_in_N & ras_in_N & cas_in_N)                                    // ref exit, pwr dn
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)               // pchg all
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)// pchg single bnk
            | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ba2_in)           // activate
            | (~rs0_in_N & ras_in_N & ~cas_in_N           & ba2_in) // xfr
            ;
//---------------------------------------
```

237. Ellsberry also discloses that the line A10 is part of the command code, as shown below. EX1037 at FIG. 8B n.3.

3. A command consists of RAS_n, CAS_n, CS, WE_n, and A(10).

238. Indeed, Ellsberry's command translation table in FIG. 8 also considers pre-charge operations in accordance with the command received on line A(10). EX1037 at FIG. 8A (reproduced below with annotations highlighting commands related to pre-charge operations). For example, Ellsberry discloses that an all-bank-precharge command is sent to both memory devices DDR A **and** DDR B, while a single-bank-precharge command is sent only to the target memory device DDR A **or** DDR B.

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2
REFRESH	X	X	X	REFRESH	X	REFRESH	X
SELF REFRESH ENTRY	X	X	X	SLF REFRESH ENTRY	X	SLF REFRESH ENTRY	X
SELF REFRESH EXIT	X	X	X	SLF REFRESH EXIT	X	SLF REFRESH EXIT	X
SINGLE BANK PRECHARGE	Col	X	X	SB PRECHG	X	SB PRECHG	X
	Row/ Bank	X	A	SB PRECHG	X	NOP	X
			B	NOP	X	SB PRECHG	X
ALL BANK PRECHARGE	X	X	X	AB PRECHG	X	AB PRECHG	X
ACTIVATE	Col	X	X	ACTIVATE	X	ACTIVATE	X
	Row/ Bank	X	A	ACTIVATE	X	NOP	X
			B	NOP	X	ACTIVATE	X
WRITE	X	X	A	WRITE	X	NOP	X
			B	NOP	X	WRITE	X
WRITE WITH AUTO PRECHARGE	Row/ Bank	X	A	WRITEAP	X	NOP	X
			B	NOP	X	WRITEAP	X
	Col	X	X	WRITEAP	X	WRITEAP	X
READ	X	X	A	READ	X	NOP	X
			B	NOP	X	READ	X
READ WITH AUTO PRECHARGE	Row/ Bank	X	A	READAP	X	NOP	X
			B	NOP	X	READAP	X
	Col	X	X	READAP	X	READAP	X

ⓐ ⓑ ⓒ ⓓ ⓔ ⓕ ⓖ ⓗ ⓘ

Fig. 8A

239. Accordingly, Ellsberry discloses to a Skilled Artisan using the transition bit Bank A(2) as well as line A10 (part of the command code) to perform rank multiplication. A Skilled Artisan would have understood this role of the line A10 for pre-charging since it is described in the JEDEC standard. *See, e.g.*, EX1029 (JESD79-2) at Table 2 and 3 (reproduced above in ¶ 234, showing the Auto precharge role of line A10) & p.49, Table 10 (reproduced in part below, annotated, showing the specific values of A10 for those pre-charge related

operations). For example, the value of the bit A10 determines whether the precharge command is directed to a single bank (A10 is Low) or to all banks (A10 is high), just like in Ellsberry and the '912 Patent's EXAMPLE 1. *Id.*

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3

240. In another implementation of Ellsberry (illustrated below), the primary address space corresponds to a single x8 DDR2 memory device with 512Mb (2 times 256Mb) capacity (red), and the memory module uses two x8 DDR2 memory devices (yellow), each having a 256Mb capacity (light green and blue) to simulate the larger capacity memory device. EX1037 at FIG. 7D (reproduced below, annotated, and with header information added from FIG. 7A).

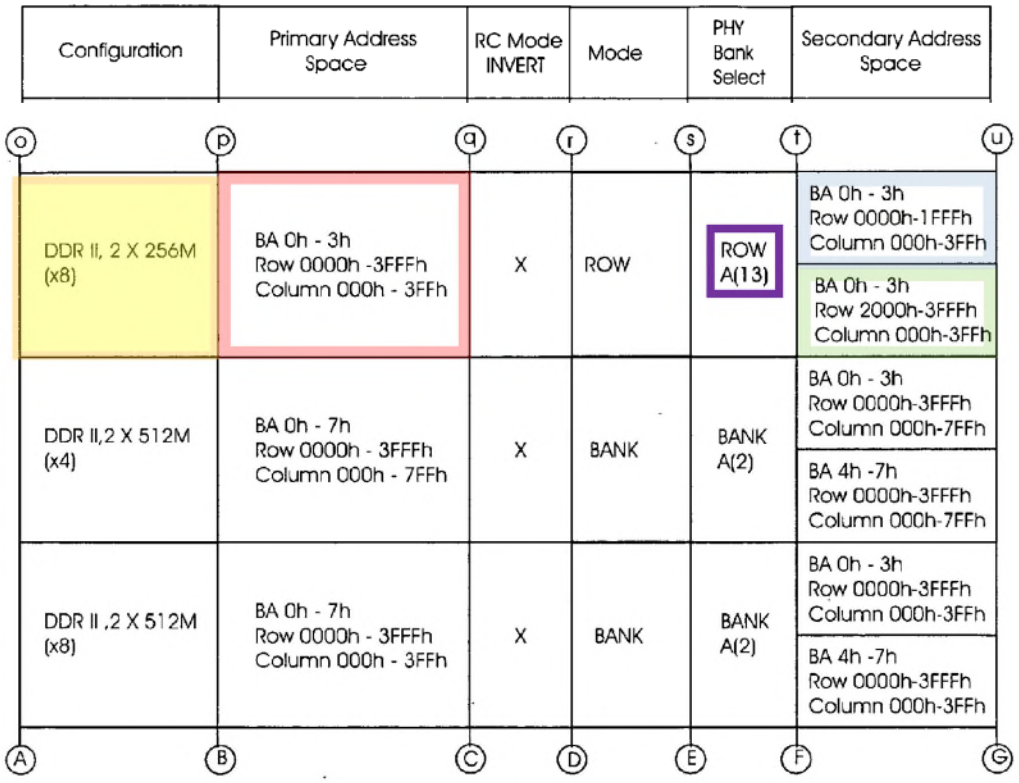


Fig. 7D

241. Similar to the previous example in Ellsberry, this example also follows the JEDEC standard's 256Mb and 512Mb addressing that differ in row address A13. EX1029 (JESD79-2) at p.7 (Tables 1 and 2 reproduced below, annotated). Furthermore, for the reasons discussed above, a Skilled Artisan would have understood that the row address bit A13 is bank specific and arrives before the read or write command, so Ellsberry's logic uses the bank address signals to properly store and retrieve the respective row address bit A13 for each activated bank. *See supra* ¶¶158-163; *see also, e.g.*, EX1044 (Dell) at 8:36-40 ("The ASIC 24 needs to store the BA1 address applicable to each of the BA0 options. This

allows the ASIC 24 to re-send the BA1 signal at CAS time to ensure that the correct bank is addressed.").

Table 1 — 256Mb Addressing

Configuration	64Mb x4	32Mb x 8	16Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A12	A0 ~ A12	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A8
Page size*1	1 KB	1 KB	1 KB

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

242. In this second exemplary implementation, Ellsberry discloses an address mapping similar to that in the "EXAMPLE 2" Verilog code in the '912 Patent describing 256Mb to 512Mb density multiplication with the transition bit being the row address bit A_{13}. EX1001 at 17:28-31 ("Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A13 density transition bit is listed below in Example 2."). And following Ellsberry's disclosure and the knowledge of a Skilled Artisan, EXAMPLE 2 uses the bank address signals (bnk0 and bnk1, brown below) to select one of four registers

(a13_00, a13_01, a13_10, a13_11, red) to store the row address bit "a13" (orange below) received with an earlier activate command (actv_cmd, blue below). *Id*. at cols. 17-18.

```
// latched a13 flags cs0, banks 0-3
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R ) // activate
  begin
        1_a13_00 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R)  // activate
  begin
        1_a13_01 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)  // activate
  begin
        1_a13_10 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)   // activate
  begin
        1_a13_11 <= a13_r ;
  end
```

The selection of the target rank, however, is based on the stored row address bit a13 (orange), not the bank address signals. *Id*. at 13:21 (Table 4, below, identifying A13 as the density transition bit for density transition from 256 Mb to 512 Mb), 17:29-31.

TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	to be determined

243. Accordingly, Ellsberry discloses "*the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,*" as recited by Claim 16.

h) *[16.c.iii]* the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,

244. Ellsberry discloses "*the circuit* [e.g., Control Unit ASIC (red below)] *generating a set of output signals*[e.g., ACA, CS0A, ACB, CS0B (blue below),] *in response to the set of input signals* [e.g., AC, CS0 (orange below)], *the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks* [e.g., two ranks 1206, 1208 (light blue, light green, below, corresponding to the chip-select signals CS0A and CS0B, respectively)]." *See, e.g.*, EX1037 at FIG. 12 (reproduced and annotated below, showing rank 1206 being controlled by CS0A and ACA, and rank 1208 controlled

by CS0B and ACB, where the input control signals are for only one rank); *see also id.* at Fig. 13 (showing four ranks, where the input control signals are for only two ranks).

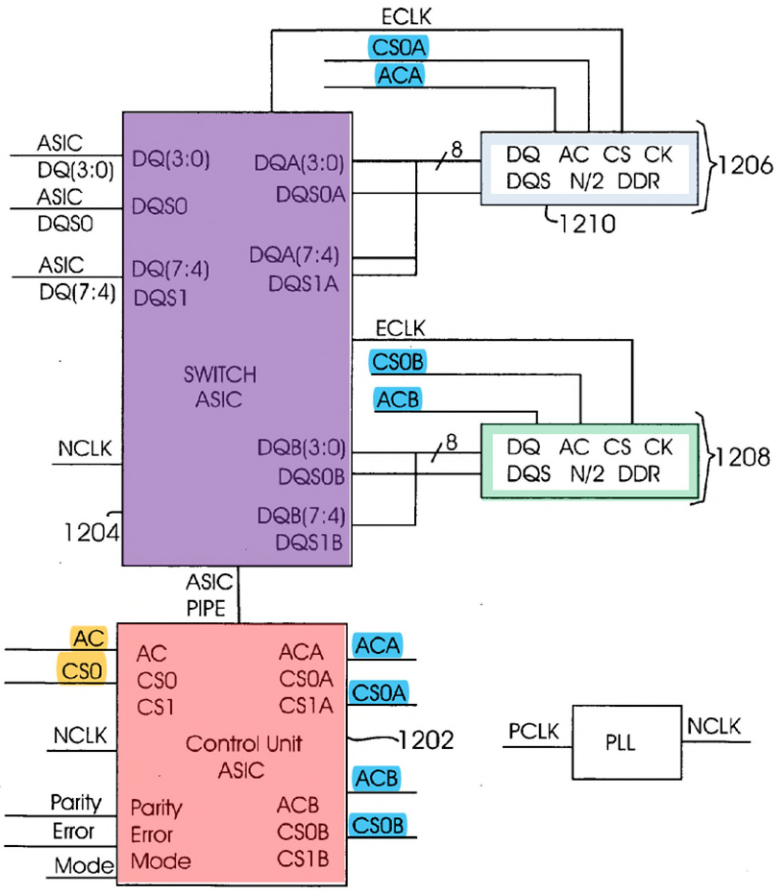


Fig. 12

245. For example, Ellsberry discloses in detail the relationship between the input command received by the Control Unit (red, above) ("*circuit*") and the commands ("*output signals*") sent by the Control Unit to the memory devices, consistent with the JEDEC standards. EX1037, *e.g.*, at [0050]&Fig. 8A (reproduced below, annotated);EX1029,6,49&n.2. As shown below, the column

on the left shows the command received by the Control Unit from the system memory controller, and the "DDR A" and "DDR B" columns on the right illustrate the commands sent to the memory device connected to Port A and Port B, respectively. *Id*. at [0042] ("In this implementation, two memory banks (i.e., DDR A and DDR B) are controlled by a control unit 204. … For example, a "WRITE" command from the control unit 204 causes a "WRITE" operation to be sent to the intended memory bank (as determined by the address mapping) and a NOP command (no operation) to be sent to the other memory bank. Thus, data is written to a memory bank (e.g., banks on DDR A) while the other memory bank (banks on DDR B) receive a NOP.").

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2
REFRESH	X	X	X	REFRESH	X	REFRESH	X
SELF REFRESH ENTRY	X	X	X	SLF REFRESH ENTRY	X	SLF REFRESH ENTRY	X
SELF REFRESH EXIT	X	X	X	SLF REFRESH EXIT	X	SLF REFRESH EXIT	X
SINGLE BANK PRECHARGE	Col	X	X	SB PRECHG	X	SB PRECHG	X
	Row/ Bank	X	A	SB PRECHG	X	NOP	X
			B	NOP	X	SB PRECHG	X
ALL BANK PRECHARGE	X	X	X	AB PRECHG	X	AB PRECHG	X
ACTIVATE	Col	X	X	ACTIVATE	X	ACTIVATE	X
	Row/ Bank	X	A	ACTIVATE	X	NOP	X
			B	NOP	X	ACTIVATE	X
WRITE	X	X	A	WRITE	X	NOP	X
			B	NOP	X	WRITE	X
WRITE WITH AUTO PRECHARGE	Row/ Bank	X	A	WRITEAP	X	NOP	X
			B	NOP	X	WRITEAP	X
	Col	X	X	WRITEAP	X	WRITEAP	X
READ	X	X	A	READ	X	NOP	X
			B	NOP	X	READ	X
READ WITH AUTO PRECHARGE	Row/ Bank	X	A	READAP	X	NOP	X
			B	NOP	X	READAP	X
	Col	X	X	READAP	X	READAP	X

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Fig. 8A

246. Ellsberry also discloses how the Control Unit ("*circuit*") maps the row, column, and bank address signals received from the system controller (primary address space, red below) to the addresses of the physical memory devices on the module (secondary address space, blue/green below) as explained above with reference to claim element [16.c.ii]. *Supra* ¶¶ 232-243; *see also* EX.1037 at [0037] ("FIGS. 7A-F illustrate an address mapping table, or bank

switch state machine, that may be used by the control unit to map a received address (primary address space) to one of the memory banks (secondary address space) according to one embodiment of the invention.") & Fig. 7 (Fig. 7D reproduced below, annotated to highlight the first and second examples discussed above).

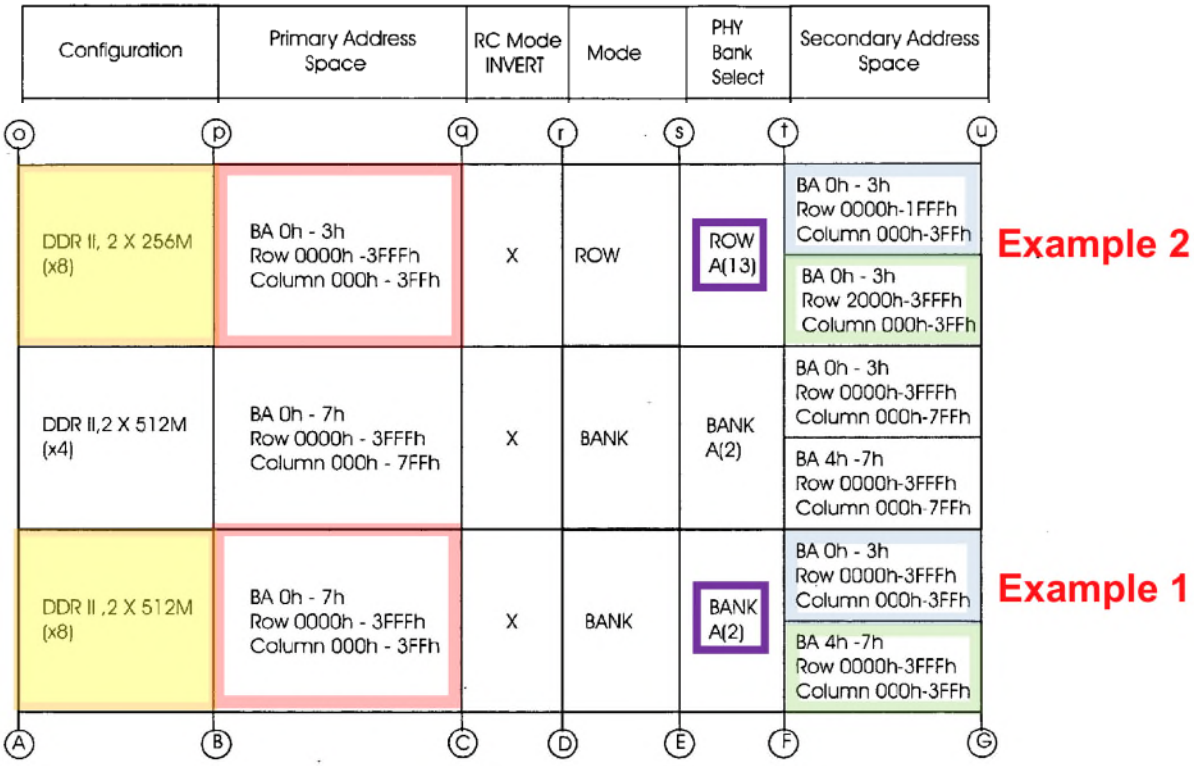

Fig. 7D

247. Thus, Ellsberry discloses "*the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,*" as recited by Claim 16.

i) *[16.c.iv]* <u>wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and</u>

248. <u>Ellsberry</u> discloses "*wherein the circuit* [e.g., Control Unit ASIC (red below)] *further responds to a command signal* [e.g., for a read or write command per the JEDEC standard, EX1029,6,49] *and the set of input signals from the computer system by selecting one or two ranks* [e.g., one rank] *of the first number of ranks* [e.g., two ranks] *and transmitting the command signal to at least one DDR memory device of the selected one or two ranks* [e.g., one rank] *of the first number of ranks* [e.g., two ranks]."

249. For example, <u>Ellsberry</u> discloses that the "control unit maps a received logical address to a physical address corresponding to the particular memory bank configuration employed. It also directs commands to the memory banks to indicate which memory bank should be operational and which one should be passive (do nothing)." EX1037 at [0011]. "Depending on which command is invoked and the memory addressing scheme used (e.g., column or row addressing), the control unit 204 operates to send either the same command [e.g., REFRESH or ALL BANK PRECHARGE below] to both memory banks (DDR A and DDR B) or different commands to each memory bank [e.g., READ or WRITE (with chip-

select asserted) to one, and NOP (with chip-select not asserted) to others, EX1029,48,49]. For example, a 'WRITE' command from the control unit 204 causes a 'WRITE' operation to be sent to the intended memory bank (as determined by the address mapping) and a NOP command (no operation) to be sent to the other memory bank. Thus, data is written to a memory bank (e.g., banks on DDR A) while the other memory bank (banks on DDR B) receive a NOP [i.e., "no operation" command, EX1029,48,49]." *Id*. at [0042], FIG. 8A (reproduced below with annotations).

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2
REFRESH	X	X	X	REFRESH	X	REFRESH	X
SELF REFRESH ENTRY	X	X	X	SLF REFRESH ENTRY	X	SLF REFRESH ENTRY	X
SELF REFRESH EXIT	X	X	X	SLF REFRESH EXIT	X	SLF REFRESH EXIT	X
SINGLE BANK PRECHARGE	Col	X	X	SB PRECHG	X	SB PRECHG	X
	Row/ Bank	X	A	SB PRECHG	X	NOP	X
			B	NOP	X	SB PRECHG	X
ALL BANK PRECHARGE	X	X	X	AB PRECHG	X	AB PRECHG	X
ACTIVATE	Col	X	X	ACTIVATE	X	ACTIVATE	X
	Row/ Bank	X	A	ACTIVATE	X	NOP	X
			B	NOP	X	ACTIVATE	X
WRITE	X	X	A	WRITE	X	NOP	X
			B	NOP	X	WRITE	X
WRITE WITH AUTO PRECHARGE	Row/ Bank	X	A	WRITEAP	X	NOP	X
			B	NOP	X	WRITEAP	X
	Col	X	X	WRITEAP	X	WRITEAP	X
READ	X	X	A	READ	X	NOP	X
			B	NOP	X	READ	X
READ WITH AUTO PRECHARGE	Row/ Bank	X	A	READAP	X	NOP	X
			B	NOP	X	READAP	X
	Col	X	X	READAP	X	READAP	X

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Fig. 8A

250. For example, the first example (512Mb to 1Gb) discussed above, *supra* ¶¶229, 233-235, corresponds to the "Bank" mode in Figure 8A above because the selection of the rank on the module depends on the bank address bit BA(2). In Bank mode, an Activate command from the system controller is sent to either DDR A (the memory device in rank A) or to DDR B (the memory device in rank B) depending on the bank address bit BA(2), while the other memory device receives a No Operation (NOP) command. *Id.*; EX1029,48,49; EX1037 at [0042]

& Fig.8A. Similarly, write and read commands are sent to either DDR A (the memory device in rank A) or to DDR B (the memory device in rank B) depending on the bank address bit BA(2), while the other memory device receives a No Operation (NOP) command. *Id.*[4]

251. I note that, in this example of Ellsberry, the selection of the target rank is based on the bank address signal while a precharge command on signal line A10 is also considered, just like in EXAMPLE 1 of the Verilog code in the '912 Patent. *See supra* ¶¶236-239. Thus, in EXAMPLE 1 of the '912 Patent, the selection of the target rank is not based on the entire claimed "*set of input signals*" which includes "*at least one row/column address signal, bank address signals, and at least one chip-select signal,*" because the selection does not depend on any "*row/column address signal*." However, to the extent it is found that EXAMPLE 1 of the '912 Patent supports this claim limitation, then Ellsberry discloses the same to a Skilled Artisan for the reasons discussed above.

252. The second example in Ellsberry (256 Mb to 512Mb) discussed above, *supra* ¶¶240-241, corresponds to the "Row" mode in Figure 8A above

[4] I note that Ellsberry also discloses that certain commands, such as Mode Register Set (MRS), Extended Mode Register Set (EMRS), and Refresh are sent to both ranks DDR A and DDR B. EX1037 at Fig.8A (first three rows).

because the selection of the rank on the module depends on row address bit A(13). EX1037 at Fig. 8A; *supra* at ¶¶240-241. In this example, the selection of the target rank is based on the row address bit which is bank specific and is stored and retrieved in accordance with the bank address signals, just like in EXAMPLE 2 of the Verilog code in the '912 Patent. *See supra* ¶242. Thus, in this EXAMPLE 2 of the '912 Patent, the selection of the target rank is not based on the entire claimed "*set of input signals*" which includes "*at least one row/column address signal, bank address signals, and at least one chip-select signal*," because the selection depend on a "*row/column address signal*," not the bank address signals (which is only used to store the row address signal). *Id*. However, to the extent it is found that EXAMPLE 2 of the '912 Patent supports this claim limitation, Ellsberry discloses the same to a Skilled Artisan for the reasons discussed above.

253. In the alternative, to the extent it is found that the claimed selection of the target rank has to depend on each element in the "*set of input signals*," including "*at least one row/column address signal, bank address signals, and at least one chip-select signal*," such an implementation would have been obvious in light of Ellsberry's disclosure. For example, a Skilled Artisan would have understood that Ellsberry's rank multiplication is not limited to the expressly disclosed examples, such as those in Fig. 7. EX1037 at Fig. 7, [0058] ("While certain exemplary embodiments have been described and shown in the

accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other changes, combinations, omissions, modifications and substitutions, in addition to those set forth in the above paragraphs, are possible. Those skilled in the art will appreciate that various adaptations and modifications of the just described preferred embodiment can be configured without departing from the scope and spirit of the invention."). Indeed, a Skilled Artisan would have understood that Ellsberry's technique can be applied using other memory devices described by the JEDEC standards. EX1029 (JESD79-2) at 7 (showing the addressing modes of different DDR SDRAM devices). For example, a Skilled Artisan would have understood at the time that the capacity of a 16-bit wide one-rank memory module including two 64Mb x8 ("by eight," i.e., eight-bit wide) DDR2 memory devices (blue box) can be doubled to look like it has one rank of two 128Mb x8 memories (red box) by using four ranks of 32Mb x16 memories (green box). *See supra* ¶¶142-151. For the reasons discussed above, such a combination using both a row address A_{13} and bank address signals, including BA2, to select the target rank would have been also obvious. *Id.*

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

254. Thus, Ellsberry discloses "*wherein the circuit further responds to command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks;*" as recited by Claim 16.

j) *[16.d]* a phase-lock loop device coupled to the printed circuit board,

255. Ellsberry discloses that its module also includes "*a phase-lock loop device coupled to the printed circuit board*." *See, e.g.*, EX1037 at [0002] & FIG. 12 (reproduced below, annotated, showing PLL, yellow, on the bottom right), FIG.13.

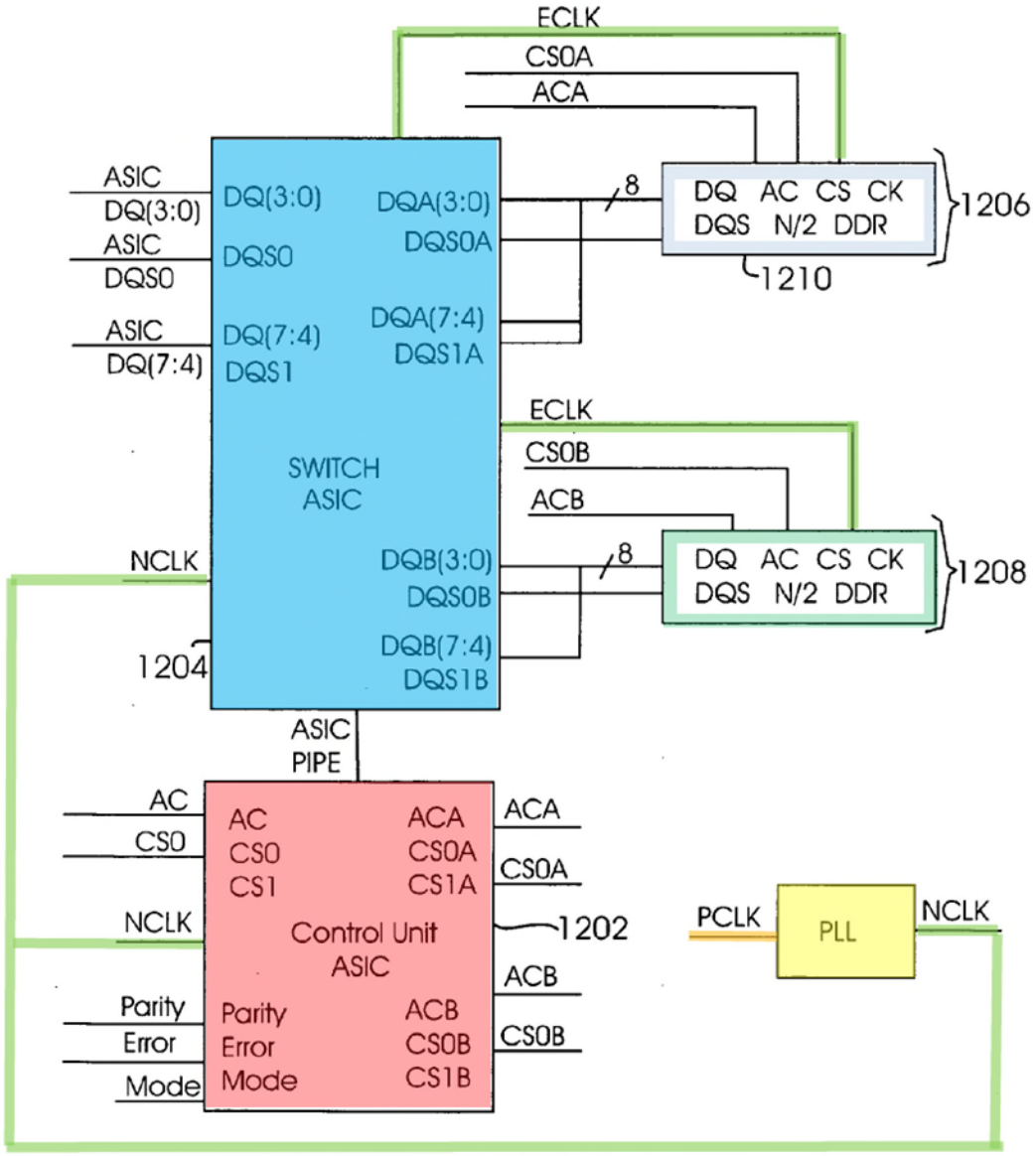

Fig. 12

256. For example, Ellsberry discloses that a "phase lock loop (PLL) 238 [(yellow)] regenerates a clock signal that can be used by the components on the memory system 200. The switch 208 may contain an internal PLL which derives the clock provided to the memory devices from the output of the external PLL 238." EX1037 at [0030] and Fig. 2 (reproduced below in part, annotated).

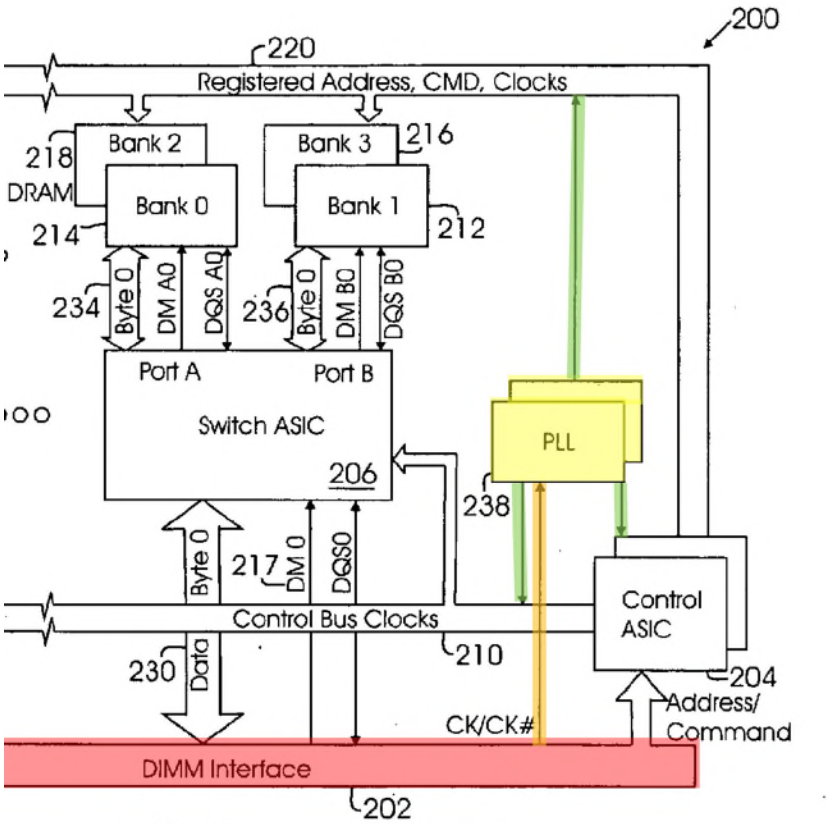

Fig. 2

257. Ellsberry also discloses that its PLL device is coupled to the circuit board. *See, e.g.*, EX1037 at Fig. 5 (reproduced below, annotated, showing PLL 514, yellow, coupled to circuit board 502 having an edge interface 506, red), [0048] ("An external phase lock loop (PLL) 514 [(yellow)] receives a clock signal [(orange line in Figs. 2 and 12 above)] from the edge interface 506 [(red)] and provides a clock signal [(green lines in Figs. 2 and 12 above)] to the memory module components"); *see also id.* [0039],[0045],[0049] & Figs. 3 and 4 (showing an embodiment of control and switch circuits 510 and 508, coupled to the circuit board 502, that also include a PLL for receiving a clock signal).

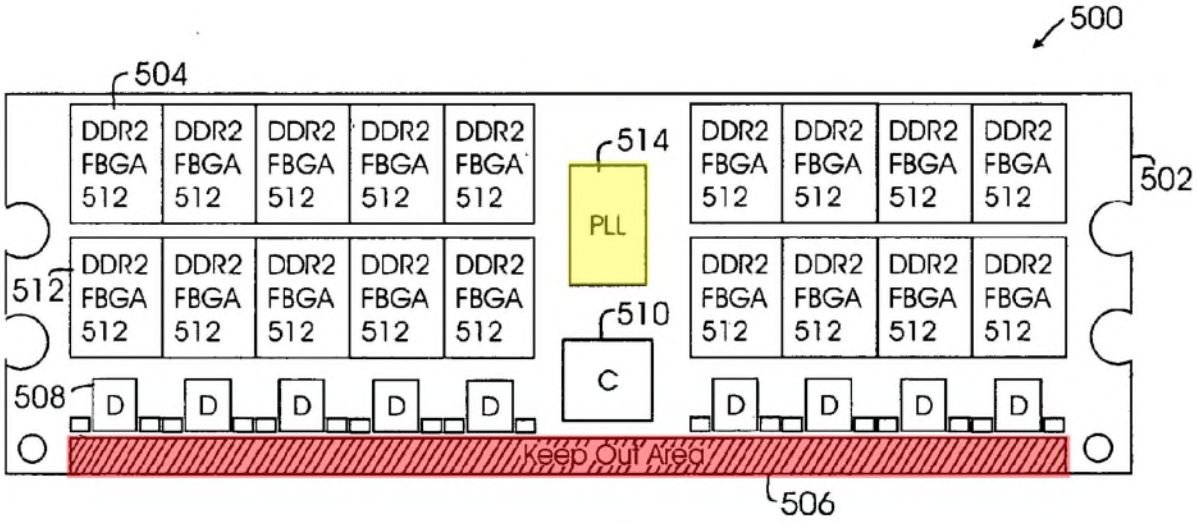

Fig. 5

258. Thus, Ellsberry discloses "*a phase-lock loop device coupled to the printed circuit board,*" as recited by Claim 16.

k) *[16.d.i]* the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

259. Ellsberry discloses to a Skilled Artisan that "*the phase-lock loop device* [e.g., as shown in FIGS. 2-5,12-13] *operatively coupled to the plurality of DDR memory devices, the logic element* [e.g., the Control Block in the Control Unit ASIC in Fig.3], *and the register* [e.g., register 302 in the Control Unit ASIC in Fig. 3]."

260. For example, as discussed above with reference to claim element **[16.d], ¶¶255-257**, Ellsberry discloses that a "phase lock loop (PLL) 238 regenerates a clock signal that can be used by the components on the memory

system 200. The switch 208 may contain an internal PLL which derives the clock provided to the memory devices from the output of the external PLL 238." EX1037 at [0030] and Fig. 2; *see also id.* Figs.3-5. As further shown in FIG. 12 of Ellsberry (reproduced below with annotations), and FIG. 13, the PLL receives a clock signal (PCLK, orange) and generates a clock signal NCLK (green), which is provided to the Control Unit ASIC (red) and to the Switch ASIC (blue). The Switch ASIC (blue), in turn, uses the clock signal NCLK (green) to derive the clock ECLK (green) provided to the memory devices (light blue, light green). Therefore, Ellsberry's PLL circuit is also operatively coupled to the plurality of DDR memory devices.

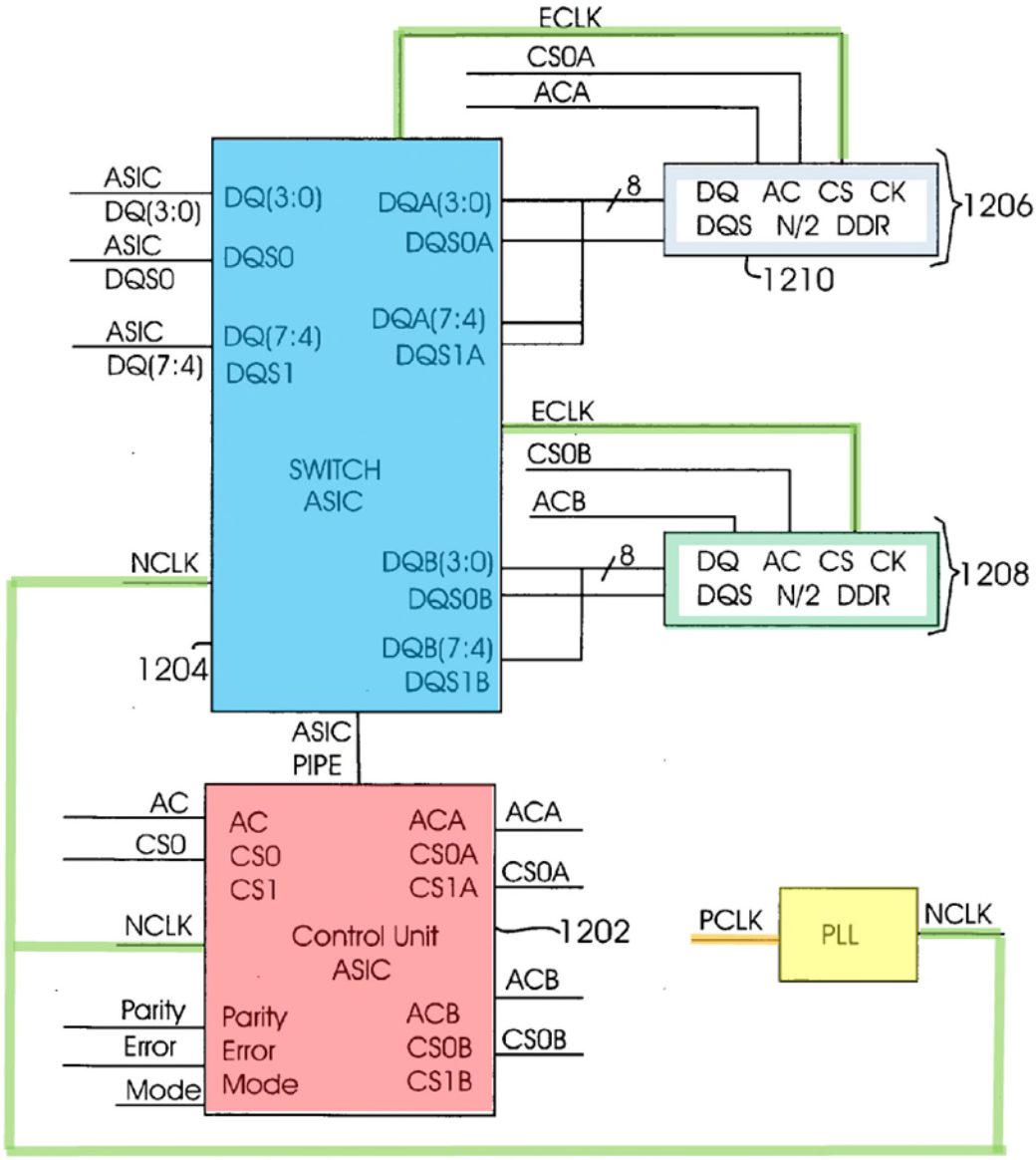
ECLK
CS0A
ACA
ASIC
DQ(3:0)
ASIC
DQS0
ASIC
DQ(7:4)
DQ(3:0)
DQS0
DQ(7:4)
DQS1
DQA(3:0)
DQS0A
DQA(7:4)
DQS1A
8
DQ AC CS CK
DQS N/2 DDR
1206
1210
ECLK
CS0B
ACB
SWITCH
ASIC
NCLK
DQB(3:0)
DQS0B
DQB(7:4)
DQS1B
8
DQ AC CS CK
DQS N/2 DDR
1208
1204
ASIC
PIPE
AC
CS0
NCLK
Parity
Error
Mode
AC
CS0
CS1
Control Unit
ASIC
Parity
Error
Mode
ACA
CS0A
CS1A
ACB
CS0B
CS1B
ACA
CS0A
1202
ACB
CS0B
PCLK
PLL
NCLK

Fig. 12

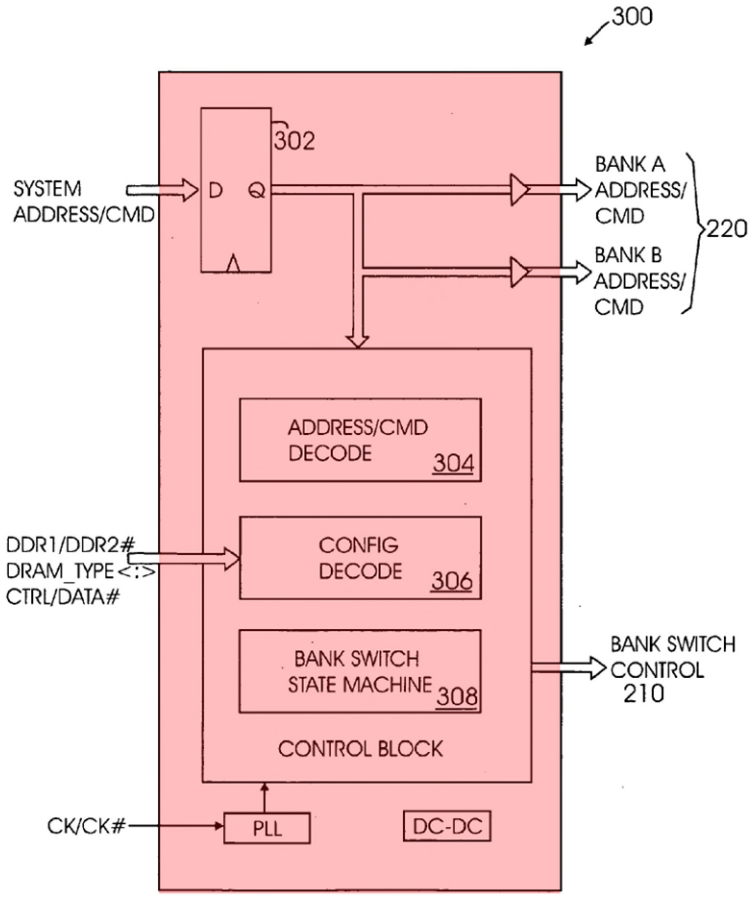

Fig. 3

261. The Control Unit ASIC (red) also uses the clock signal NCLK from the PLL to derive its own local clocks that are provided to both the Control Block and the register 302 in the Control ASIC. EX1037 at Figs. 3 (reproduced above with annotations) and 12-13.

262. To the extent one might argue that Ellsberry does not sufficiently disclose that a local clock of the Control Unit ASIC is provided to the register 302 (shown in Fig.3 above), it would have been obvious to a Skilled Artisan at the time

of Ellsberry's disclosure. A Skilled Artisan would have understood that register 302 is clocked by a local clock signal as indicated by the small triangle at the bottom of register 302. As discussed above, Ellsberry discloses that the Control Unit ASIC, which includes the register 302, receives the clock NCLK from the PLL circuit, and Ellsberry expressly teaches that "phase lock loop (PLL) 238 regenerates a clock signal that can be used by the components on the memory system 200." *Id.* at [0030]. Therefore, Ellsberry's PLL provides a clock to the Control Unit ASIC which can be used to operate its components, including the register 302. Accordingly, a Skilled Artisan would have understood and would have been motivated to use the local clock in the Control Unit ASIC to operate the register 302.

263. Thus, Ellsberry discloses "*the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,*" as recited by Claim 16.

l) [16.e] wherein the command signal is transmitted to only one DDR memory device at a time.

264. Ellsberry discloses "*wherein the command signal* [e.g., for a read or write command per the JEDEC standard, EX1029,6,49] *is transmitted to only one DDR memory device at a time*" for the reasons discussed above with reference to claim elements **[16.b.i], ¶¶214-223,** and **[16.c.iv], ¶¶248-254**. For example, in an implementation of FIG. 12 (reproduced and annotated below) an Activate, Write,

or Read command signal is transmitted to only the selected memory device, say DDR A, and the other memory device, here DDR B, receives a no-operation (NOP) command, as shown in Figure 8A below.

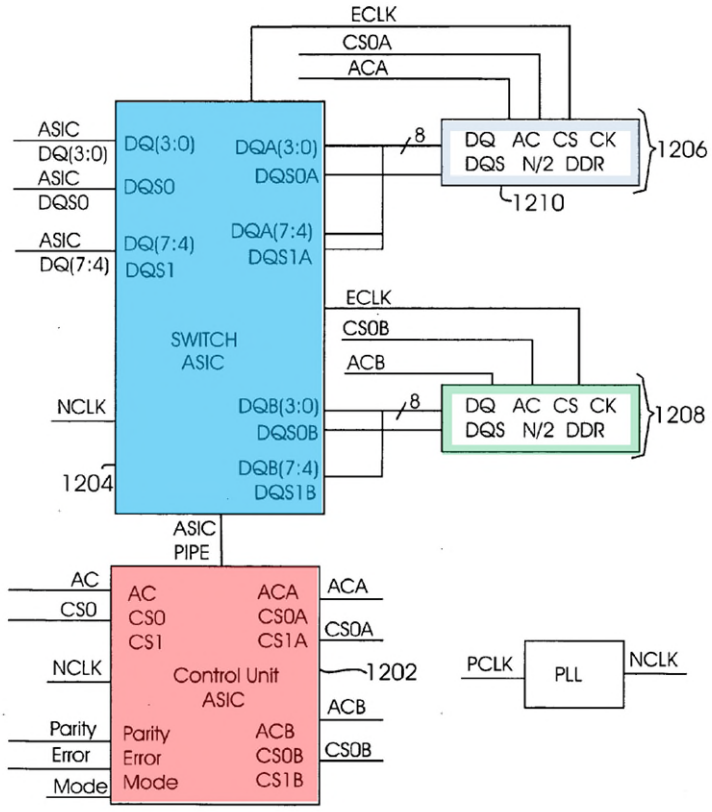

Fig. 12

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2
REFRESH	X	X	X	REFRESH	X	REFRESH	X
SELF REFRESH ENTRY	X	X	X	SLF REFRESH ENTRY	X	SLF REFRESH ENTRY	X
SELF REFRESH EXIT	X	X	X	SLF REFRESH EXIT	X	SLF REFRESH EXIT	X
SINGLE BANK PRECHARGE	Col	X	X	SB PRECHG	X	SB PRECHG	X
	Row/ Bank	X	A	SB PRECHG	X	NOP	X
			B	NOP	X	SB PRECHG	X
ALL BANK PRECHARGE	X	X	X	AB PRECHG	X	AB PRECHG	X
ACTIVATE	Col	X	X	ACTIVATE	X	ACTIVATE	X
	Row/ Bank	X	A	ACTIVATE	X	NOP	X
			B	NOP	X	ACTIVATE	X
WRITE	X	X	A	WRITE	X	NOP	X
			B	NOP	X	WRITE	X
WRITE WITH AUTO PRECHARGE	Row/ Bank	X	A	WRITEAP	X	NOP	X
			B	NOP	X	WRITEAP	X
	Col	X	X	WRITEAP	X	WRITEAP	X
READ	X	X	A	READ	X	NOP	X
			B	NOP	X	READ	X
READ WITH AUTO PRECHARGE	Row/ Bank	X	A	READAP	X	NOP	X
			B	NOP	X	READAP	X
	Col	X	X	READAP	X	READAP	X

ⓐ ⓑ ⓒ ⓓ ⓔ ⓕ ⓖ ⓗ ⓘ

Fig. 8A

See also EX1029,6,48,49; EX1038,32-37; EX1037 at [0042] ("FIGS. 8A-B illustrate a command scheme for the switch/control unit combination to operate multiple banks concurrently according to one embodiment of the invention. In this implementation, two memory banks (i.e., DDR A and DDR B) are controlled by a control unit 204. An exemplary set of memory commands and/or operations are illustrated. Depending on which command is invoked and the memory addressing

scheme used (e.g., column or row addressing), the control unit 204 operates to send either the same command to both memory banks (DDR A and DDR B) or different commands to each memory bank. For example, a 'WRITE' command from the control unit 204 causes a 'WRITE' operation to be sent to the intended memory bank (as determined by the address mapping) and a NOP command (no operation) to be sent to the other memory bank. Thus, data is written to a memory bank (e.g., banks on DDR A) while the other memory bank (banks on DDR B) receive a NOP."), [0010] ("A state machine is used to send Read/Write commands to the intended memory bank while sending no-operation commands to the other memory bank."), and [0033] ("Alternatively, when row/bank mode addressing is used, read and write commands are sent only to the targeted memory device. A NOP (no-operation) command is sent to the non-targeted memory device.").

265. Thus, Ellsberry discloses "*wherein the command signal is transmitted to only one DDR memory device at a time,*" as recited by Claim 16.

VI. SECONDARY CONSIDERATIONS

266. At this stage of these proceedings, it is my understanding that Petitioner has no burden to identify and rebut secondary considerations. Rather, it is my understanding that Patent Owner must first present a prima facie case for such consideration, which Petitioners should then have the chance to rebut. That said, I have considered evidence of secondary considerations that I am aware of at

this time, and I am currently unaware of any evidence of secondary considerations that would support a finding of non-obviousness. To the contrary, I understand that "simultaneous invention" can be a secondary consideration of obviousness. Here, as discussed above, the Ellsberry reference was filed one month before what I believe is the effective filing date of claim 16 of the '912 Patent. *See supra* ¶¶ 189-196. As discussed above, the disclosure in the Ellsberry reference not only renders claim 16 obvious in my opinion, Ellsberry's disclosure is remarkably similar to the disclosure in the '912 Patent. *See, e.g., supra* ¶¶ 236-242. I understand that such "simultaneous invention" is objective evidence of the level of skill in the art, and also objective evidence that Skilled Artisans understood both the problem and the solution to the problem. Here, in my opinion, Skilled Artisans recognized that the "problem" was that high density memory devices cost much more than low density memory devices, *see, e.g. supra* ¶ 97-98, 145, and the "solution" (and significant business opportunity) was "rank multiplication" where you replace one rank of (expensive) high-density memory devices with two or more ranks of (cheaper) low-density memory devices in a way that is transparent to the system memory controller (such that no changes are needed outside the memory module), *see id.* To give a concrete hypothetical example, if one rank of 1Gb of high-density memory cost $1,000, while two ranks of 512Mb of low-density memory cost $200, the "solution" of "rank multiplication" would present a

significant business opportunity to create a module with 1Gb of memory that cost, for example, $500 — much less than the competing 1Gb module costing $1,000, but still a significant profit margin given that the memory only cost $200. In my opinion, Amidi, Perego, and Ellsberry all recognized this "problem" (and business opportunity) and all provided very similar solutions — with Ellsberry's solution nearly identical to the solution in the '912 Patent — all in the 18-month period before the effective filing date of claim 16 of the '912 Patent. In my opinion, this is objective evidence that claim 16 of the '912 Patent was obvious.

VII. CONCLUSION

267. For all of the reasons set forth above, it is my opinion that claim 16 of the '912 Patent is invalid.

* * *

EXHIBIT LIST

Exhibit #	Reference Name
1001	U.S. Patent No. 7,619,912 with *Inter Partes* Reexamination Certificate
1002	File History of U.S. Patent No. 7,619,912
1003	Declaration of Dr. Wolfe
1004	Curriculum Vitae of Dr. Wolfe
1005	U.S. Provisional Application No. 60/588,244
1006	U.S. Provisional Application No. 60/550,668
1007	U.S. Provisional Application No. 60/575,595
1008	U.S. Patent No. 7,289,386
1009	U.S. Patent No. 7,286,436
1010	Prosecution History for *Inter Partes* Reexamination No. 95/000,578 of the ’912 Patent
1011	Decisions by the PTAB in *Inter Partes* Reexamination Nos. 95/000,578; 95/000,579; and 95/001,339 of the ’912 Patent
1012	*Inter Partes* Reexamination Certificate for the ’912 Patent (Feb. 8, 2021)
1013	Affirmance of the Examiner’s Decision on Reexamination of ’386 Patent (Feb. 25, 2015)
1014	Reexamination Certificate for ’386 Patent (Aug. 19, 2016)
1015	U.S. Patent No. 7,636,274
1016	Appeal 2017-007075 Affirmance of the Examiner’s Decision on Reexamination of ’274 Patent (May 9, 2017)
1017	Reexamination Certificate for ’274 Patent (Nov. 5, 2018)

Exhibit #	Reference Name
1018	U.S. Patent No. 7,881,150
1019	IPR2014-00882 Final Written Decision on Remand ('150 patent) (March 29, 2018)
1020	IPR2014-01011 Final Written Decision on Remand ('150 patent) (March 29, 2018)
1021	U.S. Patent No. 8,081,536
1022	IPR2014-00883 Final Written Decision on Remand ('536 patent) (March 29, 2018)
1023	IPR2015-01021 Final Written Decision ('536 patent) (Sept. 28, 2016)
1024	U.S. Patent No. 8,756,364
1025	IPR2017-00549 Final Written Decision ('364 patent) (May 3, 2018)
1026	U.S. Patent No. 7,532,537
1027	IPR2017-00667 Final Written Decision ('537 patent) (July 18, 2018)
1028	IPR2017-00668 Final Written Decision ('537 patent) (July 18, 2018)
1029	JEDEC JESD79-2 standard for DDR2 SDRAM (Sept. 2003)
1030	JEDEC JESD79 standard for DDR SDRAM (June 2000)
1031	Carlson Declaration for JESD79
1032	JEDEC JESD21-C design specification for DDR SDRAM Registered DIMM (January 2002)
1033	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008)
1034	Bruce Jacob, *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* (Dec. 10, 2002)
1035	U.S. Patent No. 7,363,422 to Perego et al.

Exhibit #	Reference Name
1036	U.S. Patent Pub. No. 2006/0117152 to Amidi et al.
1037	U.S. Patent Pub. No. 2006/0277355 to Ellsberry et al.
1038	IPR2018-00362 Final Written Decision (Patent 9,606,907) (June 27, 2019)
1039	Carlson Declaration for JESD79-2
1040	Carlson Declaration for JESD21-C
1041	U.S. Patent. No. 5,513,135 to Dell et al.
1042	J.P. 2002-184176 to Masashi
1043	Harold S. Stone, Microcomputer Interfacing (1982)
1044	U.S. Patent No. 6,209,074 to Dell et al.

CLAIM LISTING

Ref. #	Listing of Challenged Claims
[16.pre]	A memory module connectable to a computer system, the memory module comprising:
[16.a]	a printed circuit board;
[16.b]	a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,
[16.b.i]	the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
[16.c]	a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register,
[16.c.i]	the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,
[16.c.ii]	the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,
[16.c.iii]	the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,
[16.c.iv]	wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and
[16.d]	a phase-lock loop device coupled to the printed circuit board,

Ref. #	Listing of Challenged Claims
[16.d.i]	the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
[16.e]	wherein the command signal is transmitted to only one DDR memory device at a time.